QSFP-DD PCIe 5.0 DAC

0.5~2m

Black Mesh

Key Features
- Supports 8x32GT/s NRZ PCIe Gen5
- QSFP-DD x8 to QSFP-DD x8 copper cable assembly
- Single Wire Size: 28AWG
- Maximum link length up to 2m
- Maximum power consumption:<0.05W each end
- Operating temperature: 0°C to +70°C
- 3.3V Power Supply
- Hot Pluggable
- RoHS & Reach Compliance

Applications
- Gen5 x8 PCIe

Supported Standards
- QSFP-DD MSA
- PCI Express CEM Specification 5.0

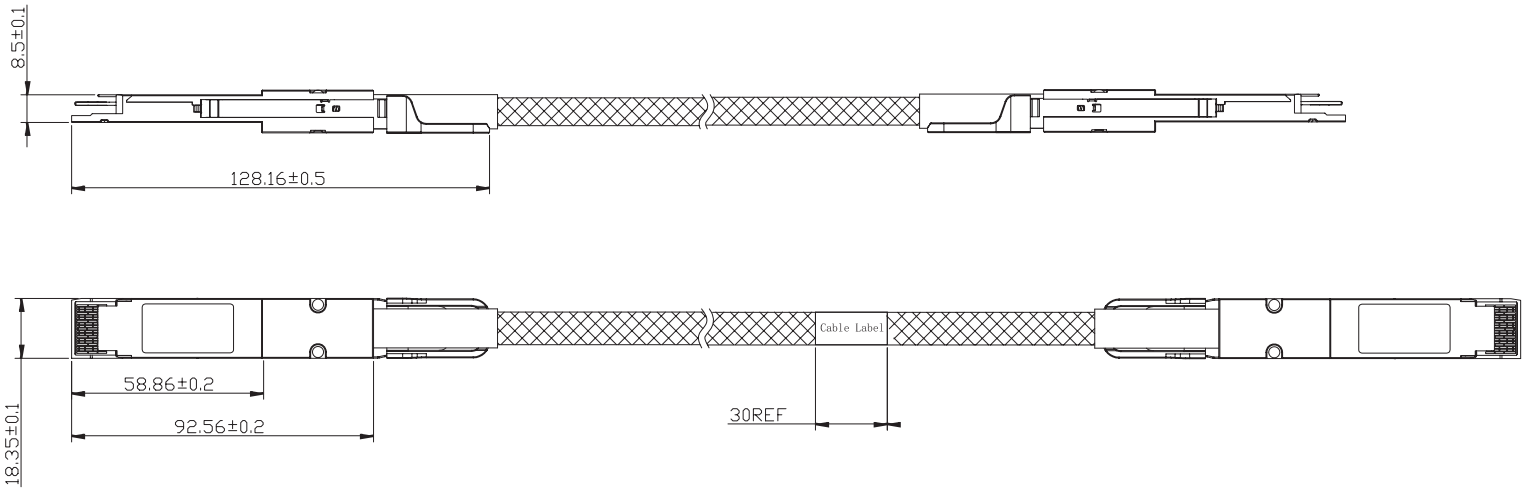
Ordering Information

L1GG-221xxxC	QSFP-DD to QSFP-DD PCIe 5.0 DAC – 0.5~2m				
Ordering P/Ns	Description	Length	AWG	Cable	NOTE
L1GG-221005C	QSFP-DD x8 to QSFP-DD x8 PCIe 5.0 DAC	0.5m	28 AWG	Black Mesh	
L1GG-221010C	QSFP-DD x8 to QSFP-DD x8 PCIe 5.0 DAC	1.0m	28 AWG	Black Mesh	
L1GG-221020C	QSFP-DD x8 to QSFP-DD x8 PCIe 5.0 DAC	2.0m	28 AWG	Black Mesh	
xxx define DAC cable length					

General Description

The QSFP-DD PCIE Direct Attach Cable product is a 8-channel parallel copper direct attach cable for storage, data center, and high performance computing connectivity. It offers 8 independent data transmission channels and 8 data receiving channels via the copper cable, the aggregate data rate of 800Gbps over 2.0 meters transmission can be achieved with this product.

Mechanical Outline



General Product Characteristics

QSFP-DD DAC Specifications	
Number of Lanes	Tx8 Rx8
Channel Data Rate	32GT/s
Operating Temperature	0 to + 70°C
Storage Temperature	-40 to + 85°C
Supply Voltage	3.3 V nominal
Electrical Interface	76 pins edge connector
Management Interface	Serial, I^2C

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1(>2000 Volts)
Electromagnetic Interference(EMI)	FCC Class B	Compliant with Standards
	CENELEC EN55022 Class B	
	CISPR22 ITE Class B	
RF Immunity	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from 80 to 1000MHz
RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives 6/6	RoHS 6/6 compliant

QSFP-DD PIN Function Definitions

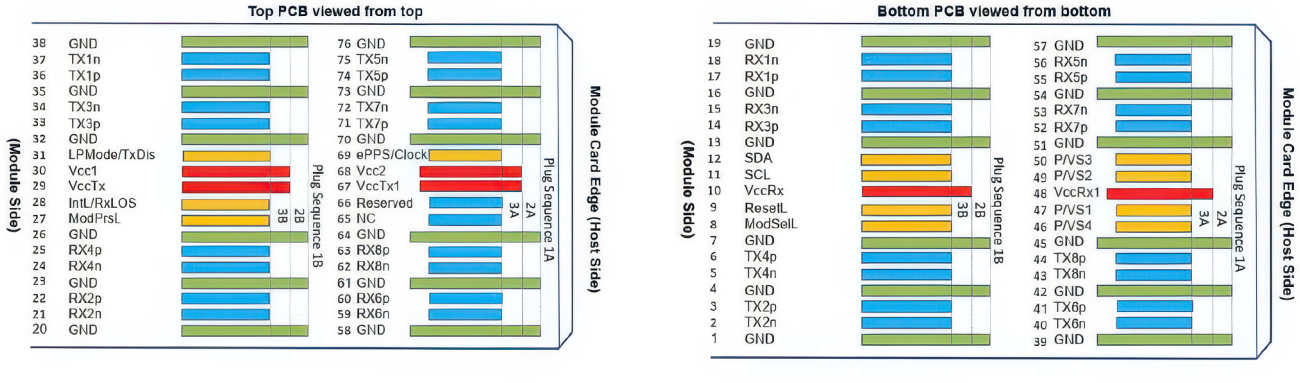
Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCOMS-I/O	SCL	TWI Serial Interface Clock
12	LVCOMS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output

25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOSL	Interrupt/optional RxLOS
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46	LVCOMS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCOMS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
48		VccRx1	3.3V Power Supply

49	LVCOMS/CML-I	P/VS2	Programmable/Module Vendor Specific 2
50	LVCOMS/CML-I	P/VS3	Programmable/Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connect
66		Reserved	For future use
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69	LVCOMS-I	ePPS/Clock	1PPS PTP clock or reference clock input
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

QSFP-DD Electrical Pad Layout

For detail mechanical information, please refer to the related document of QSFP-DD MSA.



Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

Disclaimer

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