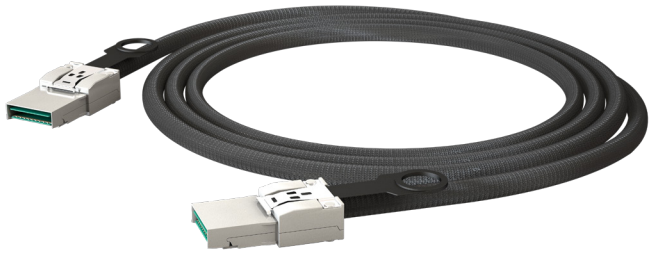
CDFP to CDFP PCIe 5.0 DAC



0.5~2m

Black Mesh

Key Features
- PCIe 5.0 CopprLink, 32 GT/s per lane, x16 lanes
- Passive CDFP x16 to CDFP x16 copper cable assembly
- Maximum link length up to 2m
- Single Wire Size: 30AWG
- Maximum power consumption: 0.125W
- Operating temperature: −40°C to +85°C
- Supply voltage: 3.3V DC
- Hot Pluggable
- RoHS & REACH Compliance
- Halogen-Free version available

Applications
- AI/ML Accelerator & GPU Interconnects
- High Performance Computing (HPC)
- PCIe 5.0 Fabric Switches & Servers
- Storage Expansion Enclosures
- Data Center & Networking Equipment

Supported Standards
- CopprLink External Cable Spec for PCIe 5.0/6.0 v0.9
- PCI Express CEM Specification 5.0 Rev 0.9
- SFF-TA-1032 Multi-Lane External High Speed Cable
- OIF-CMIS Rev 5.2

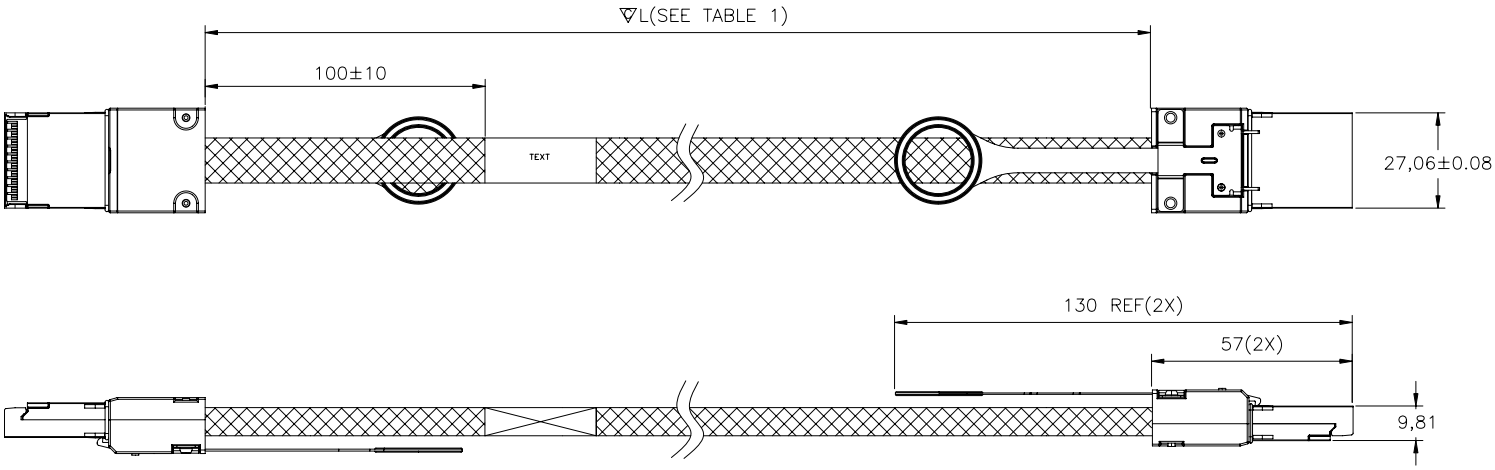
Ordering Information

L1KK-321xxxC	CDFP to CDFP PCIe 5.0 DAC – 0.5~2m				
Ordering P/Ns	Description	Length	AWG	Cable	NOTE
L1KK-321005C	CDFP x16 to CDFP x16 PCIe 5.0 DAC	0.5m	30 AWG	Black Mesh	
L1KK-321010C	CDFP x16 to CDFP x16 PCIe 5.0 DAC	1.0m	30 AWG	Black Mesh	
L1KK-321020C	CDFP x16 to CDFP x16 PCIe 5.0 DAC	2.0m	30 AWG	Black Mesh	
xxx define DAC cable length					

General Description

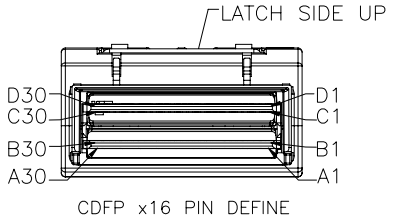
The CDFP to CDFP PCIe 5.0 DAC is a Direct Attach Copper cable designed for high-speed interconnects inside servers, HPC systems, and data center infrastructure.
It features CDFP x16 connectors on both ends and supports the CopprLink PCIe 5.0 standard, delivering 32 GT/s per lane across 16 bidirectional lanes for an aggregate bandwidth of 512 Gbps full duplex. The cable is available in lengths from 0.5 m to 2 m with 30AWG copper conductors in a black mesh jacket.
With a maximum power consumption of 0.125W per end, it supports hot-plug operation and works across a temperature range of −40°C to +85°C. It is RoHS and REACH compliant and available in a Halogen-Free version.
Typical applications include interconnects between AI/ML accelerators and GPUs, PCIe 5.0 fabric switches, high-density storage enclosures, and networking equipment in data center environments.

Mechanical Outline



General Product Characteristics

4CDFP to CDFP PCIe 5.0 DAC	Specifications
Number of Lanes	16 (x16 configuration)
Channel Data Rate	32 GT/s per lane (NRZ, PCIe 5.0)
Operating Temperature	−40°C to +85°C
Storage Temperature	−40°C to +85°C
Supply Voltage	3.3V DC
Management Interface	Serial, I^2C



Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
Supply Voltage (VCC)	−0.5	3.6	V DC	
Voltage per Signal Contact	−0.5	30	V DC	Signal only
Current per Signal Contact	—	1.0	A	
Current per Power Contact	—	1.0	A	
Operating Temperature	−40	+85	°C	Case temp.
Storage Temperature	−40	+85	°C	
Mating / Unmating Cycles	—	100	cycles	0.38 µm Au

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit	Note
Supply Voltage (VCC)	3.135	3.3	3.465	V DC	±5%
Supply Current	—	—	0.03	A	@ 3.135V
Power Consumption	—	—	0.125	W	Per end
Data Rate per Lane	—	32	—	GT/s	NRZ, PCIe 5.0
Number of Lanes	—	16	—	lanes	x16 config.
Aggregate Bandwidth	—	512	—	Gbps	Full duplex
Operating Temperature	−40	—	+85	°C	
Max Cable Length	—	—	2.0	m	
Wire Gauge	—	30	—	AWG	All lengths

Signal Integrity Performance (CopprLink PCIe 5.0/6.0 v0.9)

Parameter	Requirement	Frequency Range
Insertion Loss (SDD21)	> −5 − 0.0625·f(GHz) dB	0 – 16 GHz
Insertion Loss (SDD21)	> 5 − 1.25·f(GHz) dB	16 – 24 GHz
Return Loss (SDD11/22)	≤ −20 + 0.265·f(GHz) dB	0 – 24 GHz
PSNEXT	≤ −55 + 0.625·f(GHz) dB	0 – 24 GHz
PSFEXT	≤ −45 + 0.41667·f(GHz) dB	0 – 24 GHz
Effective Intra-Pair Skew	< 4 ps	—
Lane-to-Lane Skew	< 200 ps	—

CDFP x16 Pin Assignment — Per CopprLink PCIe 5.0/6.0 v0.9

TX (PETp/n — Transmit)	RX (PERp/n — Receive)	FLEXIO (Flexible I/O)	GND (Ground)	Power (VCC12V / Vcc3p3V)	Sideband (SCL, SDA, PERST#…)

The CDFP x16 connector has 120 contacts in 4 rows (A, B, C, D) × 30 positions. Rows A and C are dedicated GND planes (not shown). Rows B (TX) and D (RX) carry high-speed signals. Pins numbered 30→1 left-to-right as viewed from the mating face.

Root-Complex (RC) End — Fixed Connector, x16 Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Row D upper	GND	PERp11	PERn11	GND	PERp10	PERn10	GND	PERp9	PERn9	GND	PERp8	PERn8	GND	FIO7	FIO8	GND	PERp7	PERn7	GND	PERp6	PERn6	GND	PERp5	PERn5	GND	PERp4	PERn4	GND	SCL	SDA
Row D lower	GND	PERp12	PERn12	GND	PERp13	PERn13	GND	PERp14	PERn14	GND	PERp15	PERn15	GND	FIO5	FIO6	GND	PERp0	PERn0	GND	PERp1	PERn1	GND	PERp2	PERn2	GND	PERp3	PERn3	GND	3p3V	RST#
Row B upper	GND	PETp11	PETn11	GND	PETp10	PETn10	GND	PETp9	PETn9	GND	PETp8	PETn8	GND	FIO3	FIO4	GND	PETp7	PETn7	GND	PETp6	PETn6	GND	PETp5	PETn5	GND	PETp4	PETn4	GND	12V	SDA
Row B lower	GND	PETp12	PETn12	GND	PETp13	PETn13	GND	PETp14	PETn14	GND	PETp15	PETn15	GND	FIO1	FIO2	GND	PETp0	PETn0	GND	PETp1	PETn1	GND	PETp2	PETn2	GND	PETp3	PETn3	GND	2WCL	2WDA

Non-Root-Complex (NRC) End — Fixed Connector, x16 Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Row D upper	GND	PERp11	PERn11	GND	PERp10	PERn10	GND	PERp9	PERn9	GND	PERp8	PERn8	GND	FIO3	FIO4	GND	PERp7	PERn7	GND	PERp6	PERn6	GND	PERp5	PERn5	GND	PERp4	PERn4	GND	SCL	SDA
Row D lower	GND	PERp12	PERn12	GND	PERp13	PERn13	GND	PERp14	PERn14	GND	PERp15	PERn15	GND	FIO1	FIO2	GND	PERp0	PERn0	GND	PERp1	PERn1	GND	PERp2	PERn2	GND	PERp3	PERn3	GND	3p3V	RST#
Row B upper	GND	PETp11	PETn11	GND	PETp10	PETn10	GND	PETp9	PETn9	GND	PETp8	PETn8	GND	FIO7	FIO8	GND	PETp7	PETn7	GND	PETp6	PETn6	GND	PETp5	PETn5	GND	PETp4	PETn4	GND	12V	PR/PE
Row B lower	GND	PETp12	PETn12	GND	PETp13	PETn13	GND	PETp14	PETn14	GND	PETp15	PETn15	GND	FIO5	FIO6	GND	PETp0	PETn0	GND	PETp1	PETn1	GND	PETp2	PETn2	GND	PETp3	PETn3	GND	2WCL	2WDA

Note:
Rows A and C are fully dedicated to GND and are not shown in the pin maps above. All 30 positions in Rows A and C are GND. FIOx = FLEXIOx; RST# = PERST#; 12V = VCC12V; 3p3V = Vcc3p3V. Source:CopprLink External Cable Specification for PCIe 5.0 and 6.0 v0.9.

Sideband Signal Definitions

Signal	Direction	Type	Function
PERST#	RC → NRC	Sideband	PCIe fundamental reset signal (active low). Issued by Root Complex.
SCL	RC → NRC	I²C	Management I²C clock line (OIF-CMIS). 100 kHz / 400 kHz.
SDA	Bidirectional	I²C	Management I²C data line (OIF-CMIS).
2WCL	RC → NRC	2-Wire	Alternate 2-wire management clock (secondary management bus).
2WDA	Bidirectional	2-Wire	Alternate 2-wire management data (secondary management bus).
FLEXIO1–8	Vendor-defined	Flexible I/O	Optional vendor-defined sideband signals. FLEXIO numbering mirrors between RC and NRC ends.
VCC12V	—	Power	12V auxiliary power supply contact.
Vcc3p3V	—	Power	3.3V auxiliary power supply contact.
PR/PE	NRC end only	Sideband	Presence / Power Enable detect signal. Present at NRC end only (replaces SDA at B29 RC).

Note: Rows A and C are fully dedicated to GND and are not shown in the pin maps above. All 30 positions in Rows A and C are GND.
Source: CopprLink External Cable Specification for PCIe 5.0 and 6.0 v0.9.

CDFP DAC Cable — CMIS Memory Map (Lower Memory Map, Bytes 0–255, PCIe 5.0)

Address (Decimal)	Code (Hex)	Parameter	Value / Description	Note
0	25	Identifier	CDFP (x16 PCIe)	23 = CDFP x4 PCIe 24 = CDFP x8 PCIe 25 = CDFP x16 PCIe
1	50	Version ID	CMIS 5.0	
2	80	Module Capabilities	Flat_mem, CLEI present, TWI Maximum Speed	Only page 00h implemented Module supports up to 400 kHz
3	03	Module State	ModuleLowPwr state	Interrupt not asserted (de-fault)
4–7	00	Lane Flag Summary	—	
8–13	00	Module-Level Flags	—	
14–25	00	Module-Level Monitors	—	
26–30	00	Reserved Area	—	
31–36	00	Module-Level Flag Masks	—	
37–38	00	CDB Status Area	—	
39–40	00	Module Firmware Version	—	
41–63	00	Reserved	—	
64–82	00	Custom Area	—	
83–84	00	Inactive Firmware Version	—	
85	03	Module Type Encodings	Passive Cu	
86	71	ApSelCode 1: Host Electrical Interface Code	PCIe 5.0	
87	01	ApSelCode 1: Module Media Interface Code	Copper cable	
88	88	ApSelCode 1: Host/Media LaneCount	Host 8 lanes / Media 8 lanes	
126	00	Bank Select Byte	—	
127	00	Page Select Byte	—	
128	25	Identifier	CDFP (x16 PCIe)	23 = CDFP x4 PCIe 24 = CDFP x8 PCIe 25 = CDFP x16 PCIe
129–144	A/R	Vendor Name	—	Left-aligned, padded with ASCII spaces (20h)
145–147	70 B3 D5	Vendor OUI	—	
148–163	A/R	Vendor Part Number	—	Left-aligned, padded with ASCII spaces (20h) See Table 1(a)
164–165	41 30	Vendor Revision	—	
166–181	A/R	Vendor Serial Number	ZLYYWWDLSSSSS	Left-aligned, padded with ASCII spaces (20h) See Table 1(b)
182–189	A/R	Date Code	YYMMDD	Left-aligned, padded with ASCII spaces (20h)

190–199	00	CLEI Code	—
200–201	00	Module Power Class and Max Power	0x00
202	A/R	Cable Assembly Length	Length multiplier field / Base length field
203	23	Media Connector Type	No separable connector
204	A/R	Copper Cable Attenuation @ 5 GHz	Depends on P/N
205	A/R	Copper Cable Attenuation @ 7 GHz	Depends on P/N
206	A/R	Copper Cable Attenuation @ 12.9 GHz	Depends on P/N
207	A/R	Copper Cable Attenuation @ 25.8 GHz	Depends on P/N
208–209	00	Reserved	—
210	00	Near End Implementation	Copper cable unequalized
211	02	Implemented Lanes — Far End	—
89	01	ApSelCode 1: Host Lane Assignment	00000001
90	FF	ApSelCode 2: Host Electrical Interface Code	—
91–117	00	SFF-8024 Host/Media Advertisement	Per CMIS
118–125	00	Password Entry and Change	—

A/R = As Required (application-specific value). Bytes marked 00 are reserved or zero by default per CMIS 5.0. This table covers the Lower Memory Map only (bytes 0–127) and Lower Page 00h (bytes 128–255).

Disclaimer

Images are for illustrative purposes only and may not accurately represent the actual product. Specifications and appearances are subject to change without prior notice.

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