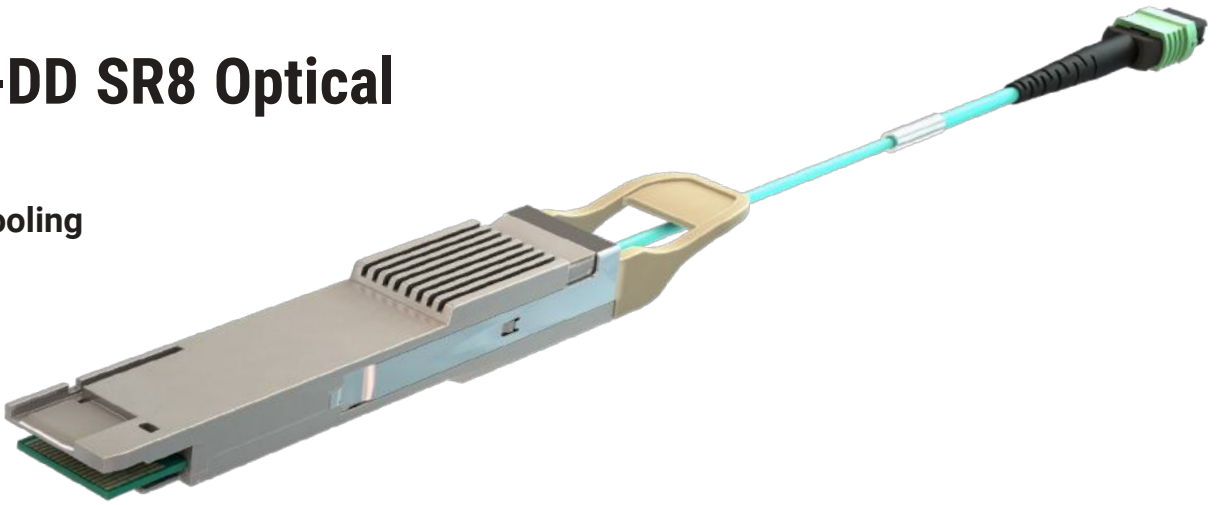
800G QSFP-DD SR8 Optical Transceiver

Module for liquid cooling



Key Feature

- 8 channels full-duplex transceiver modules
- Transmission data rate up to 106.25G per channel
- 8x106.25Gbps PAM4 transmitter and PAM4 receiver
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Power consumption <13.5W
- Hot-Pluggable QSFP-DD form factor and Compliant with CMIS
- Maximum link length of 60m on OM3 Multimode Fiber (MMF) and 100m on OM4 MMF with FEC
- MPO16 APC pigtail
- Built-in digital diagnostic functions
- Operating case temperature: Commercial (0°C to +70°C)
- 3.3V power supply voltage
- RoHS compliant(lead free)

Applications

- IEEE 802.3db 2 x 400GBASE-SR4 Ethernet (PAM4)
- The transceiver is designed for Ethernet, Telecom and Infiniband use cases
- Especially designed for liquid immersion cooling environments

Ordering Information - 800G QSFP-DD SR8 liquid immersion transceiver

Part No.	Data Rate	Distance	Wavelength	Media	Connector	Temp.
LIGM-QMSxxxC	800G	~100m	850nm	MMF	MPO-16 APC	C

Product Description

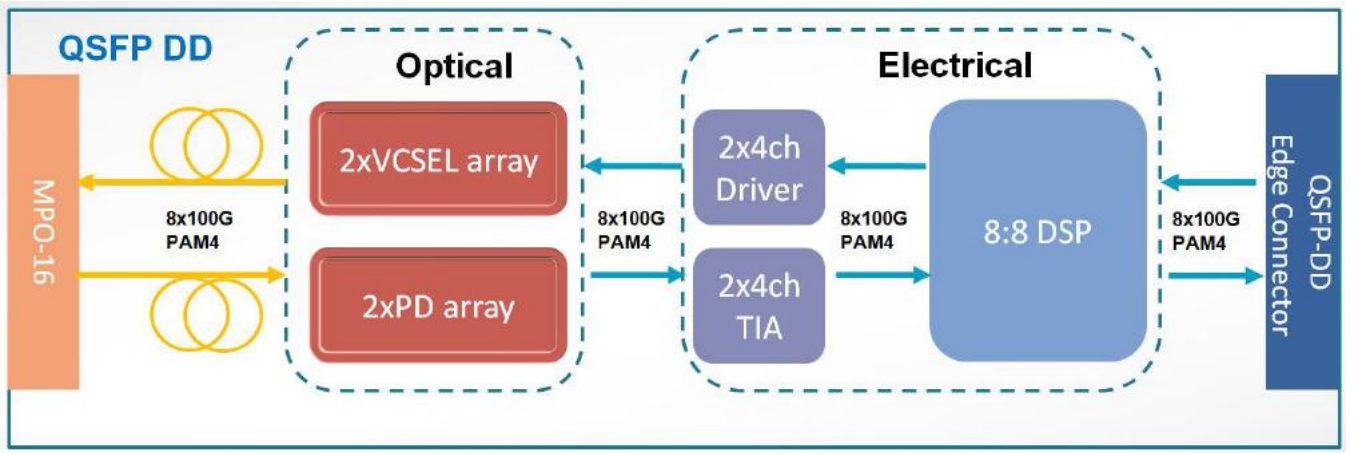
The 800G QSFP-DD SR8 is an eight-channel, pluggable, parallel fiber-optic transceiver designed for 800 Gigabit Ethernet applications, including operation in liquid immersion environments.

This high-performance transceiver is optimized for short-reach, multi-lane data communication and interconnection applications. It integrates eight transmit and eight receive data lanes, each operating at 53.125 GBd (PAM4), providing an aggregate data rate of up to 800 Gbps. Each lane supports a data rate of 106.25 Gbps and enables transmission distances of up to 60 m over OM3 multimode fiber or up to 100m over OM4 multimode fiber when Forward Error Correction (FEC) is used.

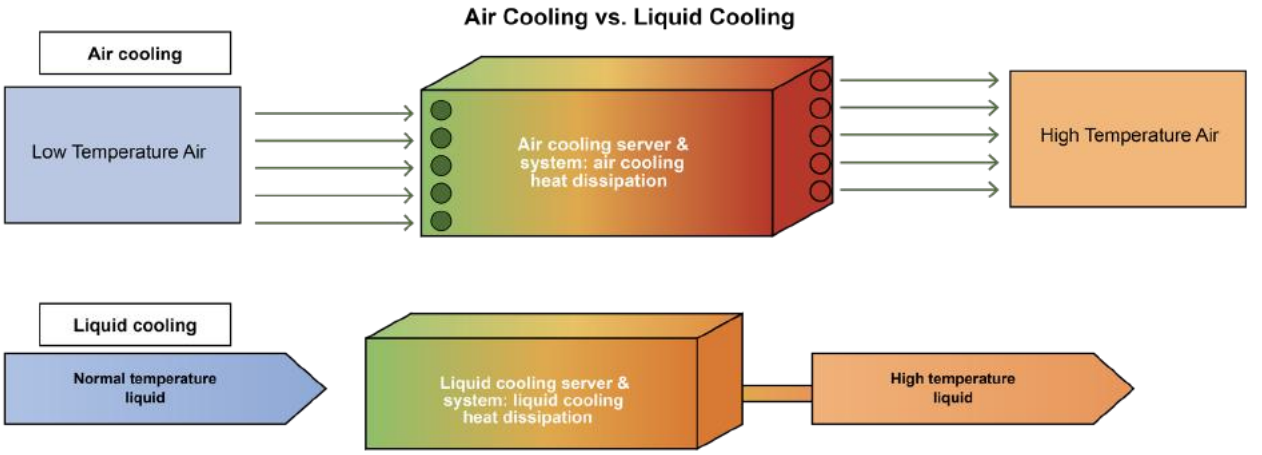
The module operates at a nominal wavelength of 850 nm over multimode fiber and uses an MPO-16 optical pigtail interface. It is compliant with the Common Management Interface Specification (CMIS) for QSFP-DD modules.

Designed with proven VCSEL-based optical technology and high-reliability electronic circuitry, this transceiver delivers robust performance, long operational lifetime, and consistent, dependable operation in demanding data center environments.

Module Block Diagram



Liquid cooling advantage



Liquid Immersion Cooling Applications

As data traffic continues to grow and the heat generated by high-performance processors and AI accelerators increases, conventional air-cooling solutions are reaching their practical limits. Liquid cooling technologies provide a more efficient method of heat removal by using dielectric fluids with high thermal capacity, significantly improving cooling efficiency and reducing overall data center power consumption.
This optical transceiver is specifically designed for operation in liquid immersion cooling environments, providing reliable performance even when fully immersed at depths of up to 10 meters. It is ideally suited for liquid-cooled servers, switches, and high-performance computing systems. The module is compatible with a wide range of dielectric immersion fluids, including fluorinated fluids and mineral oils, ensuring long-term reliability and stable optical performance in demanding immersion cooling applications.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%
Fiber Bend Radius	Rb	3		cm
Liquid immersion depth			10	m

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	ºC
Data Rate Per Lane			106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		13	13.5	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔVin	400		900	mVp-p
Differential output voltage	ΔVout			850	mVp-p
Bit Error Rate	BER			2.4E-4	
Input Logic Level High	VIH	2.0		Vcc	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	Vcc-0.5		Vcc	V
Output Logic Level Low	VOL	0		0.4	V
Input Logic Level High	VIH	2.0		Vcc	V

Notes:

1. BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	844	850	863	nm	
RMS spectral width	Δλ			0.6	nm	
Average launch power, each lane	Pout	-4.6		4	dBm	
Optical Modulation Amplitude (OMAouter), each lane	OMA	-2.6		3.5	dBm	
Transmitter and dispersion eye closure for PAM4(TDECQ),each lane	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5			dB	
Average launch power of OFF transmitter, each lane				-30	dB	
Receiver						
Centre Wavelength	λc	842	850	948	nm	
Receiver Sensitivity (OMAouter)	RXsen			max (-4.6,TECQ 6.4)	dBm	1
Stressed Receiver Sensitivity (OMAouter)	SRS			-2	dBm	2
Maximum Average power at receiver , each lane input, each lane				4	dBm	
Minimum Average power at receiver , each lane		-6.4			dBm	
Receiver Reflectance				-15	dB	
LOS Assert	LOSA	-15		-8.5	dBm	
LOS De-Assert	LOSD			-6.5	dBm	
LOS Hysteresis	LOSH	0.5			dB	

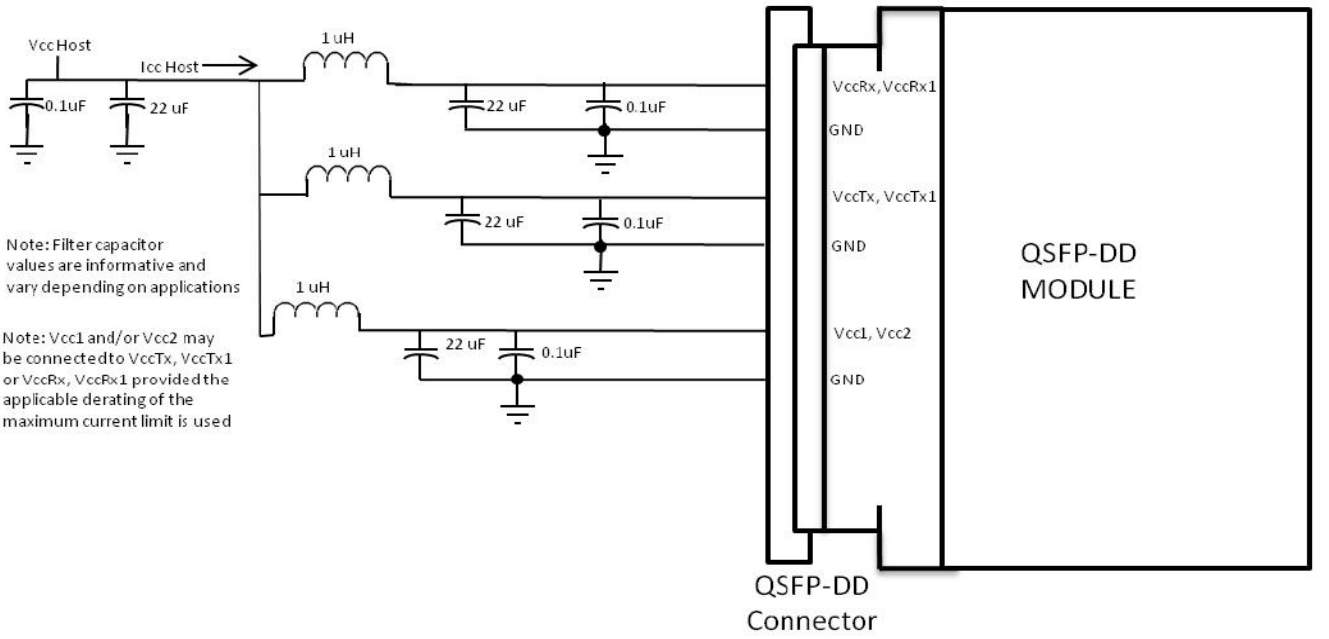
Notes:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specification

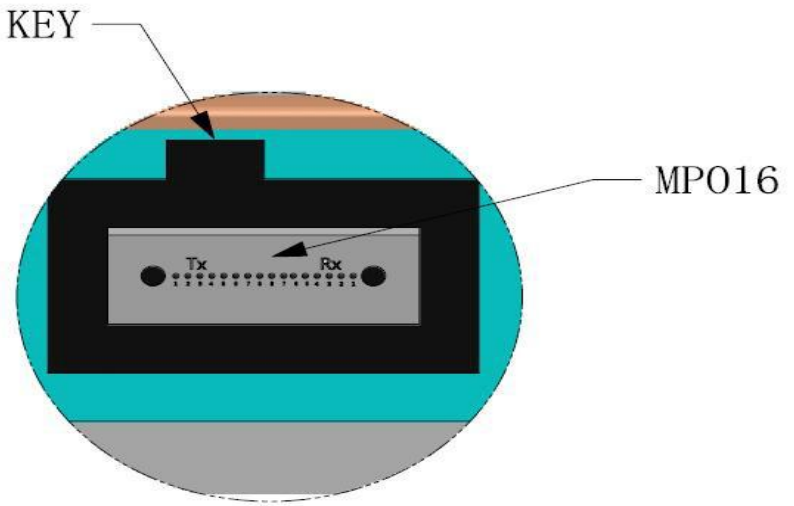
Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

Host Board Power Supply Filtering



Optical Interface Lanes and Assignment

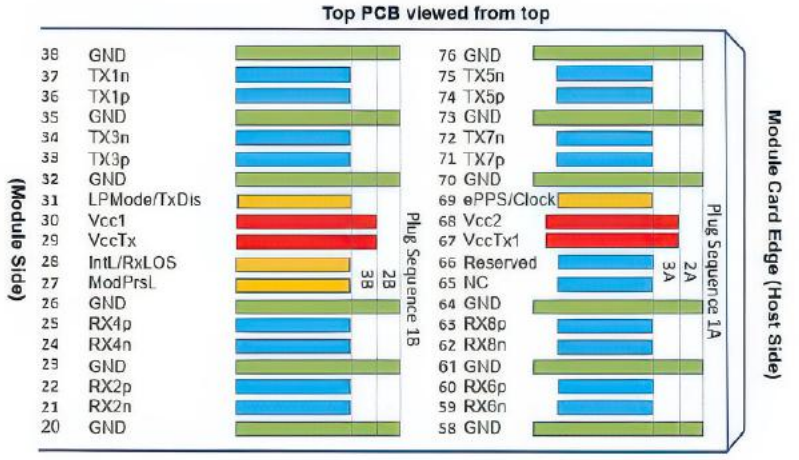
The optical interface is provided through an MPO-16/APC pigtail connector. The transmit (Tx) and receive (Rx) optical lanes shall occupy the positions illustrated in the figure below.

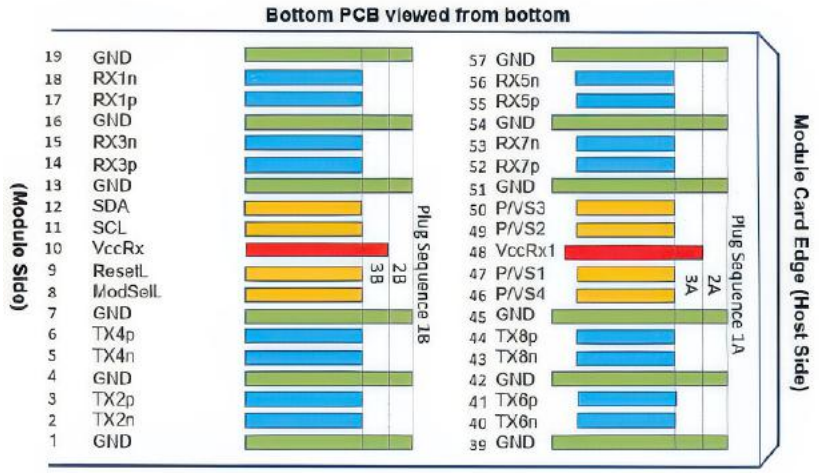


Note: The MPO-16/APC pigtail uses the opposite key orientation compared to a standard 800G QSFP-DD SR8 transceiver to ensure correct mating.

QSFP-DD Electrical Pad Layout

For detail mechanical information, please refer to the related document of QSFP-DD MSA.





QSFP-DD PIN Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCOMS-I/O	SCL	TWI Serial Interface Clock	3B	
12	LVCOMS-I/O	SDA	TWI Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1

24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RxLOSL	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power Supply Transmitter	2B	2
30		Vcc1	+3.3V Power Supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCOMS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	3
47	LVCOMS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49	LVCOMS/CML-I	P/VS2	Programmable/Module Vendor Specific 2	3A	3
50	LVCOMS/CML-I	P/VS3	Programmable/Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	

53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1B	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCOMS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

ModSelL Pin

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode Pin

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode. See CMIS Section 6.3.1.3.

ModPrsL Pin

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL Pin

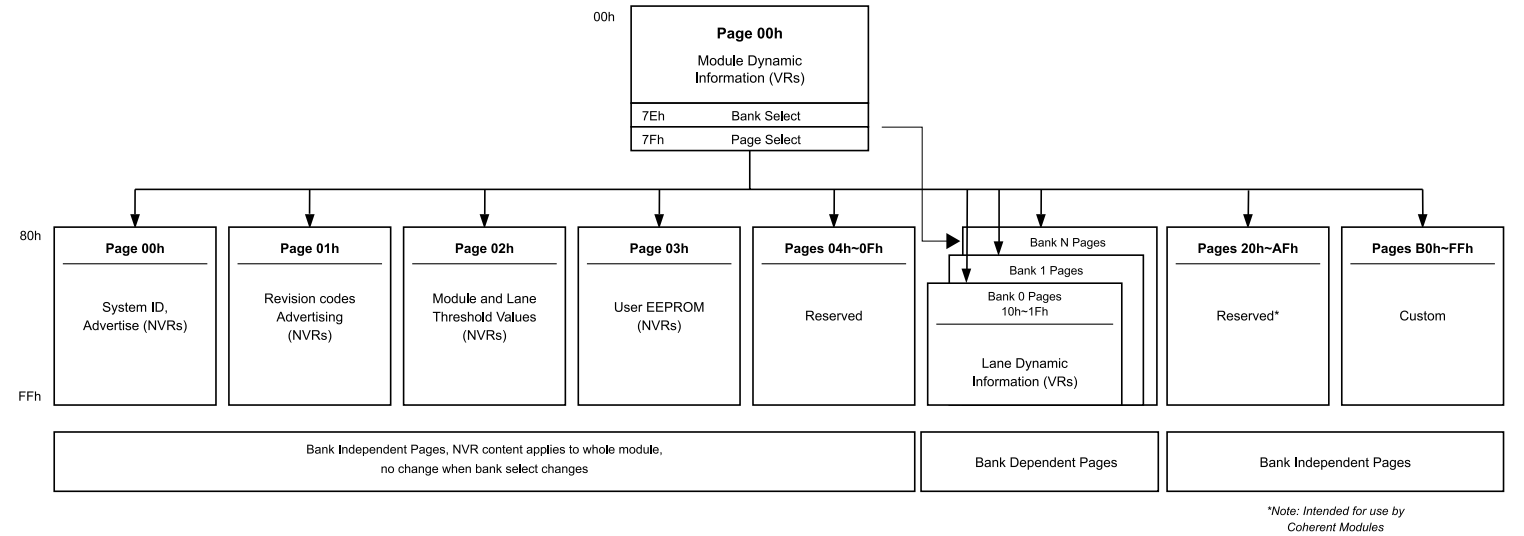
IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

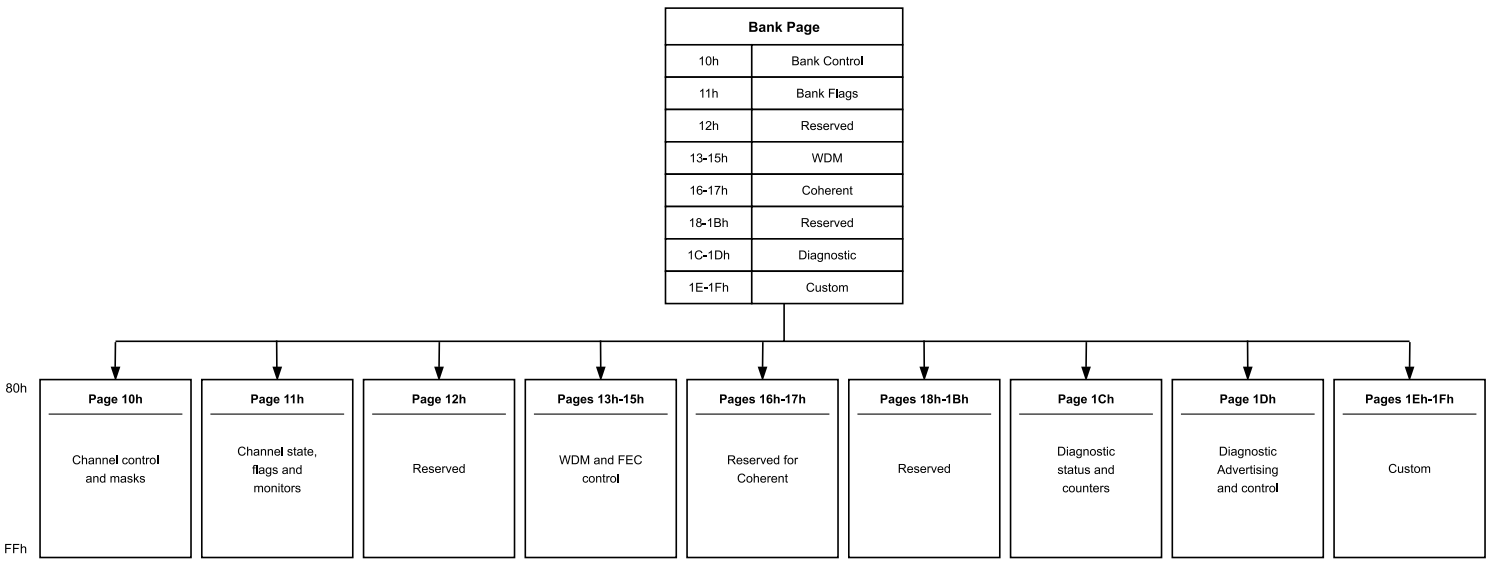
Memory Map Structure

Support for the Lower Memory and Page 00h is mandatory for all modules, including passive copper cables; therefore, these memory areas are always implemented.

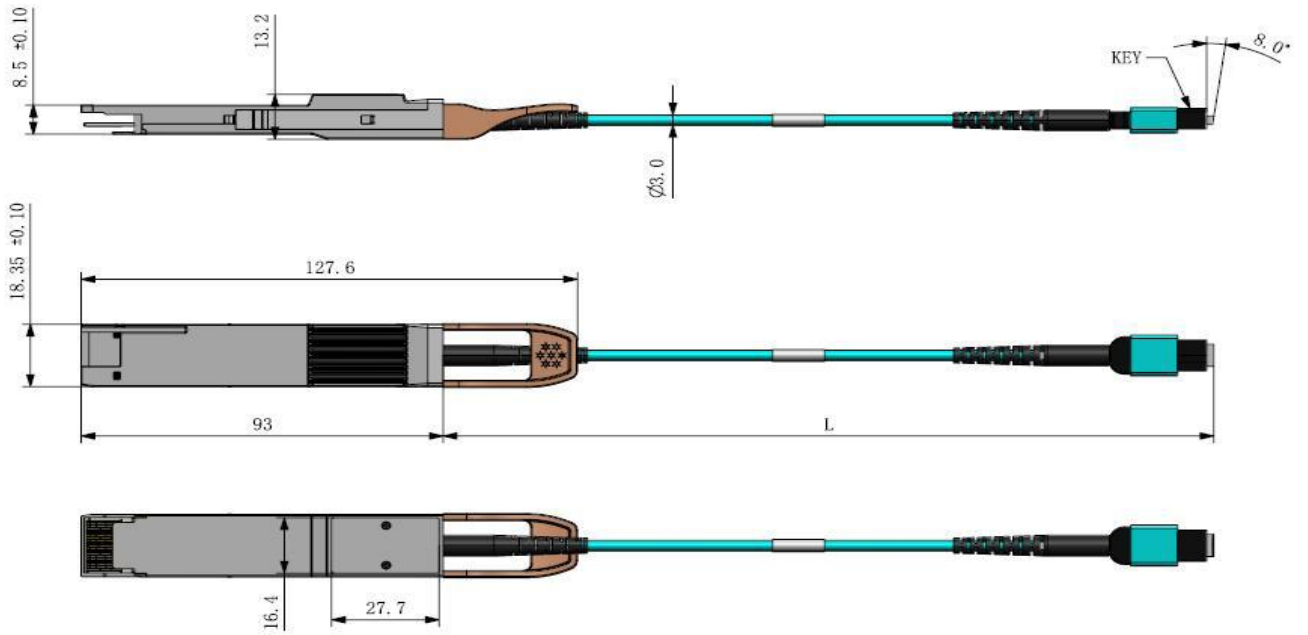
For modules supporting paged memory, implementation of Pages 01h, 02h, and Bank 0 of Pages 10h and 11h is also mandatory. Bank 0 of Pages 10h–1Fh contains lane-specific registers for the first eight lanes, while each additional bank provides support for an additional group of eight lanes. However, the allocation of information across banks may vary depending on the page and is not necessarily organized in groups of eight lanes.

This memory structure provides a scalable addressing scheme, allowing the address space to be expanded through the implementation of additional pages and banks as required by specific module types and future feature enhancements.





Mechanical Dimensions(mm)



Regulatory Compliance

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

Laser Safety Warning

This product is classified as a Class 1 Laser Product according to IEC 60825-1.
It complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007.

Caution: Use of optical instruments with this product will increase eye hazard. Do not view the laser beam directly with optical instruments or naked eyes.

Disclaimer

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