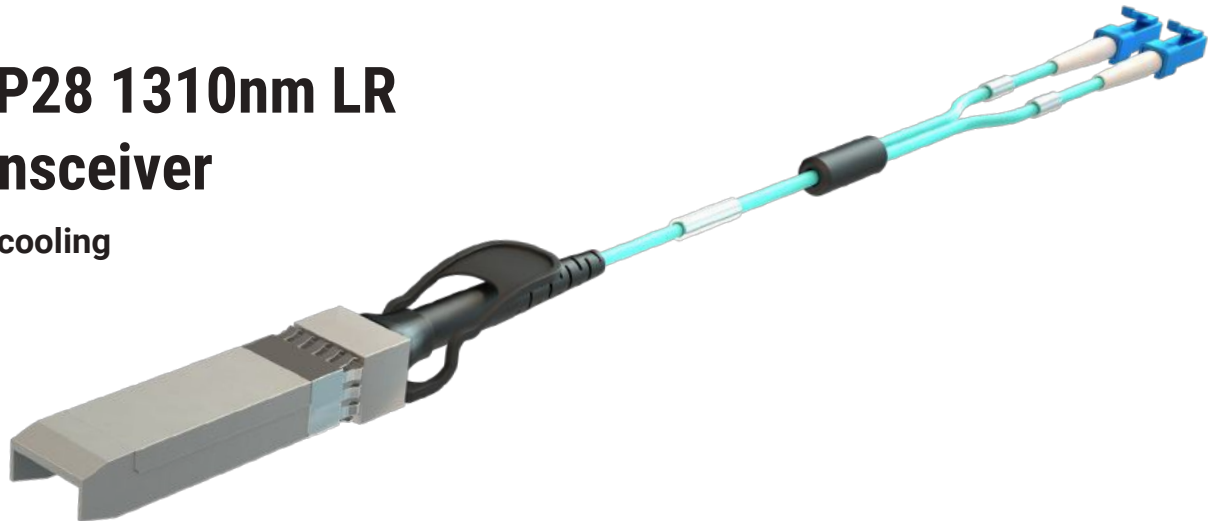




# 25Gbps SFP28 1310nm LR Optical Transceiver

Module for liquid cooling



## Key Feature

- Hot-pluggable SFP28 form factor
- Supports 25Gbps data rate
- Maximum link length of 10km
- Uncooled 1310nm DML transmitter and PIN receiver
- Internal CDR on both Transmitter and Receiver channel
- Optional pigtail type and length
- Single 3.3V power supply
- Power dissipation < 1.5W
- RoHS compliant (2011/65/EU, lead free)
- Operating case temperature range: 0°C to 60°C

## Applications

- 25GBASE-LR Ethernet
- CPRI Option 10
- Support 10G CPRI option 8 by CDR bypass
- Especially design for liquid immersion environment

## Ordering Information - 25Gbps SFP28 LR Optical Transceiver

| Part No.     | Data Rate | Distance | Wavelength | Media | Connector         | Temp. |
|--------------|-----------|----------|------------|-------|-------------------|-------|
| LIPX-UULxxxC | 25G       | ~10Km    | 1310nm     | SMF   | LC/FC/MPO Pigtail | C     |

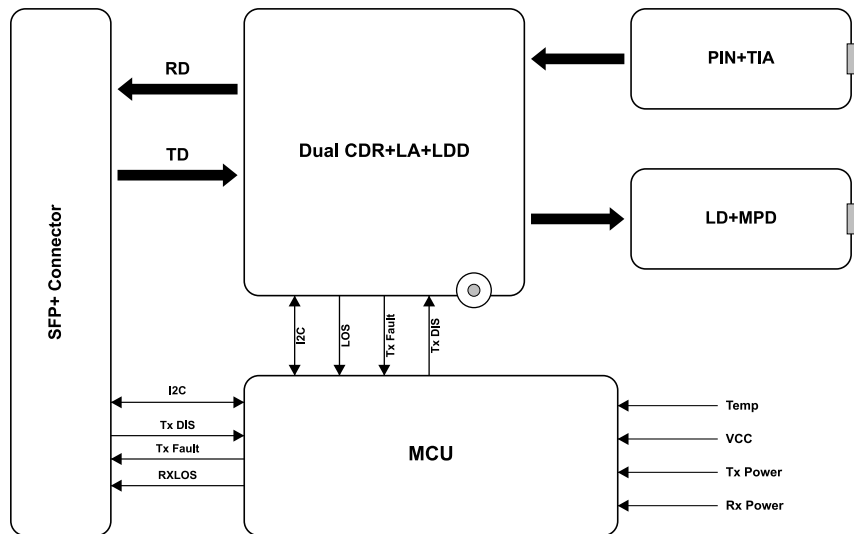
## Product Description

The Lumulus Immersion SFP28 transceiver is a single-channel, pluggable fiber optic module designed for 25 Gigabit Ethernet and CPRI Option 10 applications. Engineered specifically for reliable operation in liquid immersion environments, it delivers high performance for data communication and interconnect applications at data rates up to 25.78125 Gbps over distances of up to 10 km.

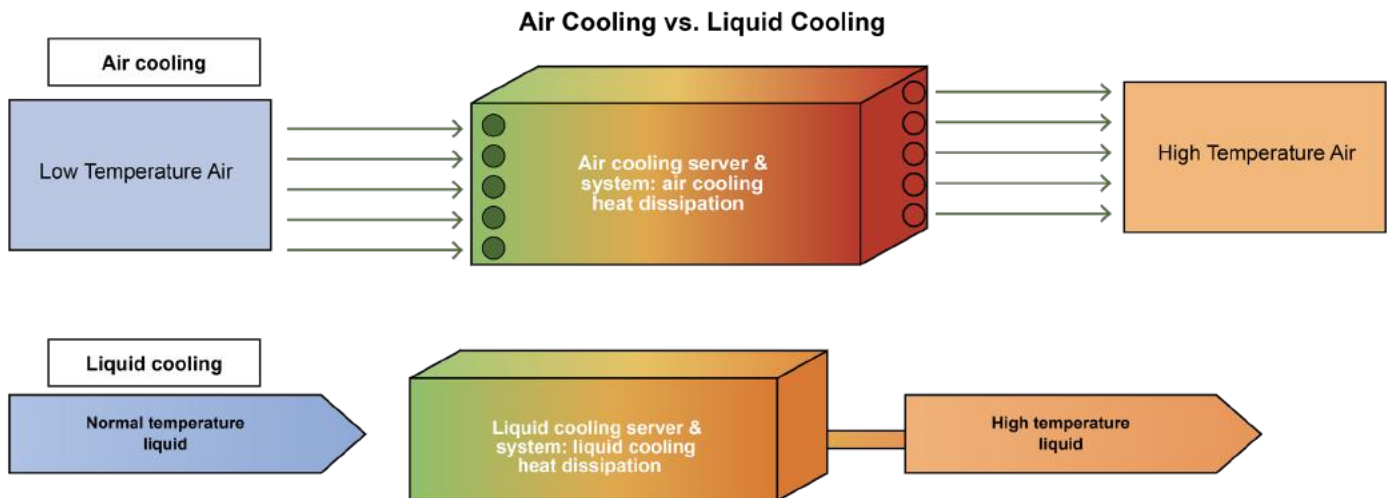
The module operates over single-mode fiber using a nominal wavelength of 1310 nm and features a standard 20-contact edge connector electrical interface. An optional pigtail optical interface is also available to support specific deployment requirements. Designed with high-quality components and proven engineering, the module provides long-term reliability, consistent performance, and dependable operation in demanding data center environments.



## Module Block Diagram



## Liquid cooling advantage



## Liquid Immersion Cooling Applications

As data traffic continues to grow and the heat generated by high-performance processors and AI accelerators increases, conventional air-cooling solutions are reaching their practical limits. Liquid cooling technologies provide a more efficient method of heat removal by using dielectric fluids with high thermal capacity, significantly improving cooling efficiency and reducing overall data center power consumption.

This optical transceiver is specifically designed for operation in liquid immersion cooling environments, providing reliable operation when fully immersed in dielectric cooling fluids at depths of up to 10 meters. It is ideally suited for liquid-cooled servers, switches, and high-performance computing systems. The module is compatible with a wide range of dielectric cooling fluids, including fluorinated fluids and mineral oils, ensuring long-term reliability and stable optical performance in demanding immersion cooling applications.



## Absolute Maximum Ratings

| Parameter           | Symbol | Min | Max | Unit |
|---------------------|--------|-----|-----|------|
| Supply Voltage      | Vcc    | 0   | 3.6 | V    |
| Storage Temperature | Ts     | -40 | 85  | °C   |
| Operating Humidity  | Rh     | 5   | 85  | %    |

## Recommended Operating Conditions

| Parameter                  | Symbol | Min  | Typical | Max  | Unit |
|----------------------------|--------|------|---------|------|------|
| Operating Case Temperature | Tc     | 0    |         | +60  | °C   |
| Power Supply Voltage       | Vcc    | 3.13 | 3.3     | 3.47 | V    |
| Power Supply Current       | Icc    |      |         | 450  | mA   |
| Liquid immersion depth     |        |      |         | 10   | m    |

## Electrical Specifications

| Parameter                                          | Symbol           | Min     | Typical | Max  | Unit  |
|----------------------------------------------------|------------------|---------|---------|------|-------|
| Differential Input Impedance                       | Zin              | 90      | 100     | 110  | ohm   |
| Differential Output Impedance                      | Zout             | 90      | 100     | 110  | ohm   |
| Differential Input Voltage Amplitude <sup>1</sup>  | $\Delta V_{in}$  | 300     |         | 1100 | mVp-p |
| Differential Output Voltage Amplitude <sup>2</sup> | $\Delta V_{out}$ | 500     |         | 800  | mVp-p |
| Input Logic Level High                             | VIH              | 2.0     |         | Vcc  | V     |
| Input Logic Level Low                              | VIL              | 0       |         | 0.8  | V     |
| Output Logic Level High                            | VOH              | Vcc-0.5 |         | Vcc  | V     |
| Output Logic Level Low                             | VOL              | 0       |         | 0.4  | V     |

Notes:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.



### Optical Characteristics

| Parameter                          | Symbol      | Min                                | Typical | Max   | Unit | Notes |
|------------------------------------|-------------|------------------------------------|---------|-------|------|-------|
| Transmitter                        |             |                                    |         |       |      |       |
| Data rate                          | BR          |                                    | 25.78   |       | Gbps |       |
| Centre Wavelength                  | $\lambda_c$ | 1295                               | 1310    | 1325  | nm   |       |
| Spectral Width (-20dB)             | $\sigma$    |                                    |         | 1     | nm   |       |
| Side Mode Suppression Ratio        | SMSR        | 30                                 |         |       | dB   |       |
| Average Output Power               | Pavg        | -7                                 |         | 2     | dBm  |       |
| Optical Modulation Amplitude       | OMA         | -4                                 |         | 2.2   | dBm  |       |
| Extinction Ratio                   | ER          | 3.5                                |         |       | dB   |       |
| Eye Mask Coordinates               |             | {0.31, 0.4, 0.45, 0.34, 0.38, 0.4} |         |       |      |       |
| Receiver                           |             |                                    |         |       |      |       |
| Data rate                          | BR          |                                    | 25.78   |       | Gbps |       |
| Centre Wavelength                  | $\lambda_c$ | 1295                               | 1310    | 1325  | nm   |       |
| Average Power at Receiver          |             |                                    |         | 2     | dBm  |       |
| Receive reflectance(max)           |             |                                    |         | -26   | dB   |       |
| Receiver Sensitivity (OMA)         | Psens       |                                    |         | -12.0 | dBm  | 1     |
| Stressed receiver sensitivity(OMA) |             |                                    |         | -9.5  | dBm  | 2     |
| LOS De-Assert                      | LOSD        |                                    |         | -12   | dBm  |       |
| LOS Assert                         | LOSA        | -30                                |         |       | dBm  |       |
| LOS Hysteresis                     |             | 0.5                                |         |       | dB   |       |

Notes:

- For 25G-LR with FEC, receiver sensitivity is defined at  $5E^{-5}$  BER level, not  $10^{-12}$  BER level.
- Measured with conformance test signal at TP3 for BER=5E-5.

### Timing and Electrical Specifications

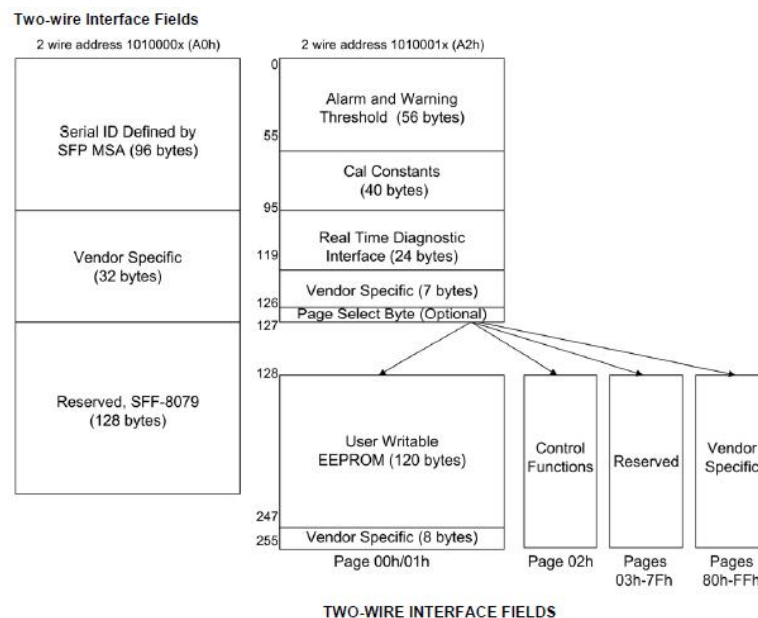
| Parameter                           | Symbol        | Min. | Max. | Unit    | Conditions                                                                                                                                                                                                                                                         |
|-------------------------------------|---------------|------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Tx_Disable assert time              | t_off         |      | 100  | $\mu$ s | Rising edge of Tx_Disable to fall of output signal below 10% of nominal                                                                                                                                                                                            |
| Tx_Disable negate time              | t_on          |      | 2    | ms      | Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.                                                                                                            |
| Time to initialize 2-wire interface | t_2w_start_up |      | 300  | ms      | From power on or hot plug after the supply meeting Table 8.                                                                                                                                                                                                        |
| Time to initialize                  | t_start_up    |      | 300  | ms      | From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational. |



|                                                                                         |                    |     |    |                                                                                                                                                                                                                                                                                                                                          |
|-----------------------------------------------------------------------------------------|--------------------|-----|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Time to initialize cooled module and time to power up a cooled module to Power Level II | t_start_up_cooled  | 90  | s  | From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational |
| Time to Power Up to Level II                                                            | t_power_level2     | 300 | ms | From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational                                                                                                                                                                                                                            |
| Time to Power Down from Level II                                                        | t_power_down       | 300 | ms | From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements                                                                                                                                                                                                                      |
| Tx_Fault assert                                                                         | Tx_Fault_on        | 1   | ms | From occurrence of fault to assertion of Tx_Fault                                                                                                                                                                                                                                                                                        |
| Tx_Fault assert for cooled module                                                       | Tx_Fault_on_cooled | 50  | ms | From occurrence of fault to assertion of Tx_Fault                                                                                                                                                                                                                                                                                        |
| Tx_Fault Reset                                                                          | t_reset            | 10  | μs | Time Tx_Disable must be held high to reset Tx_Fault                                                                                                                                                                                                                                                                                      |
| RS0, RS1 rate select timing for FC                                                      | t_RS0_FC, t_RS1_FC | 500 | μs | From assertion till stable output                                                                                                                                                                                                                                                                                                        |
| RS0, RS1 rate select timing non FC                                                      | t_RS0, t_RS1       | 24  | ms | From assertion till stable output                                                                                                                                                                                                                                                                                                        |
| Rx_LOS assert delay                                                                     | t_los_on           | 100 | μs | From occurrence of loss of signal to assertion of Rx_LOS                                                                                                                                                                                                                                                                                 |
| Rx_LOS negate delay                                                                     | t_los_off          | 100 | μs | From occurrence of presence of signal to negation of Rx_LOS                                                                                                                                                                                                                                                                              |

## Memory Organization

The transceiver provides serial ID memory contents and diagnostic information about its current operating conditions through a 2-wire serial interface (SCL and SDA). The memory map and its specific data fields are defined as follows.





## CDR Rate Select control

The Soft RS0 Select bit (A2h, byte 110, bit 3) and Soft RS1 Select bit (A2h, byte 118, bit 3) are CDR control bits that enable CDR Rate Select through the 2-wire serial interface. These bits operate in conjunction with the corresponding hardware Rate Select pins (RS0 and RS1) through a logical OR function. As a result, the CDR Rate Select is enabled whenever either the corresponding software bit is set to "1" or the associated hardware pin is driven High.

## RETIMER/CDR RATE SELECT LOGIC TABLE

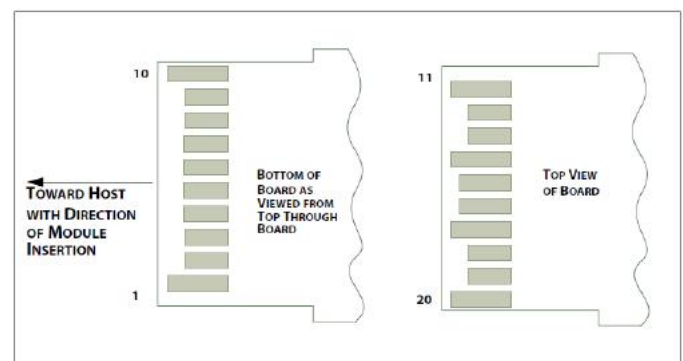
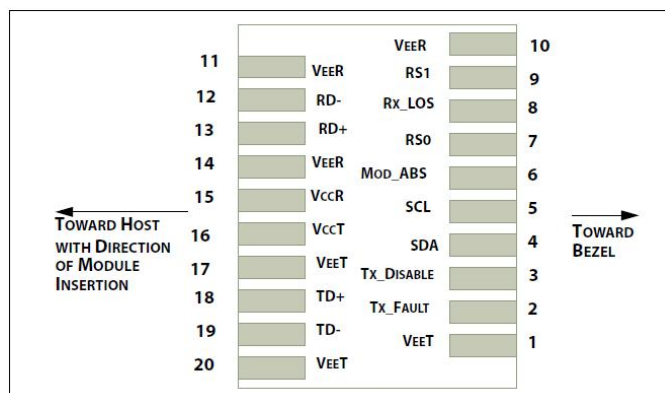
When byte 13d of A0h is set to 0Eh and bit 64.3 of A0h is set to 1

| Logic OR of RS0 pin and RS0 bit | Logic OR of RS1 pin and RS1 bit | Receiver retimer/CDR  | Transmitter retimer/CDR |
|---------------------------------|---------------------------------|-----------------------|-------------------------|
| Low/0                           | Low/0                           | Lock at low bit rate  | Lock at low bit rate    |
| Low/0                           | High/1                          | Lock at high bit rate | Bypass                  |
| High/1                          | Low/0                           | Bypass                | Bypass                  |
| High/1                          | High/1                          | Lock at high bit rate | Lock at high bit rate   |

Note: Low and high bit rates are defined in byte 13d of A0h.

## SFP28 Electrical Pad Layout

For detail mechanical information, please refer to the related document of SFP MSA.

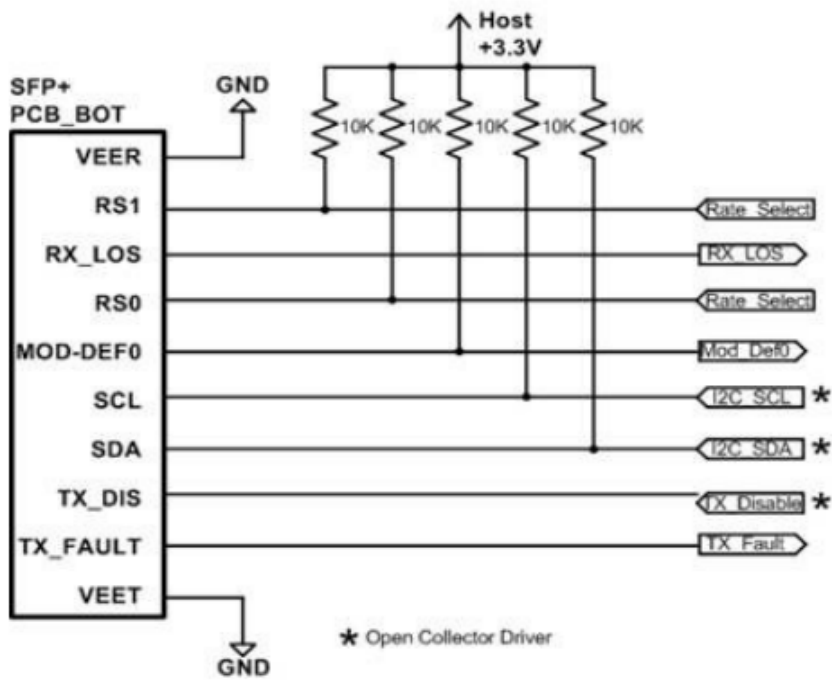
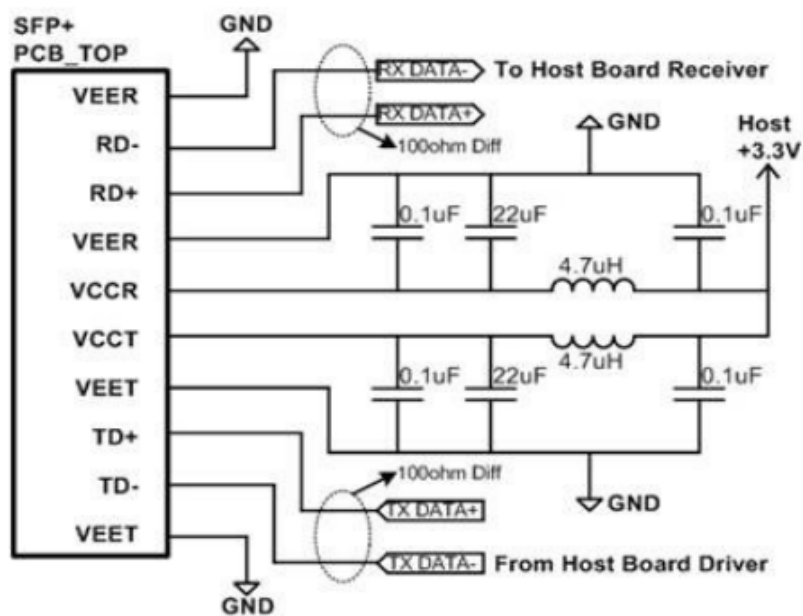




## SFP28 PIN Function Definitions

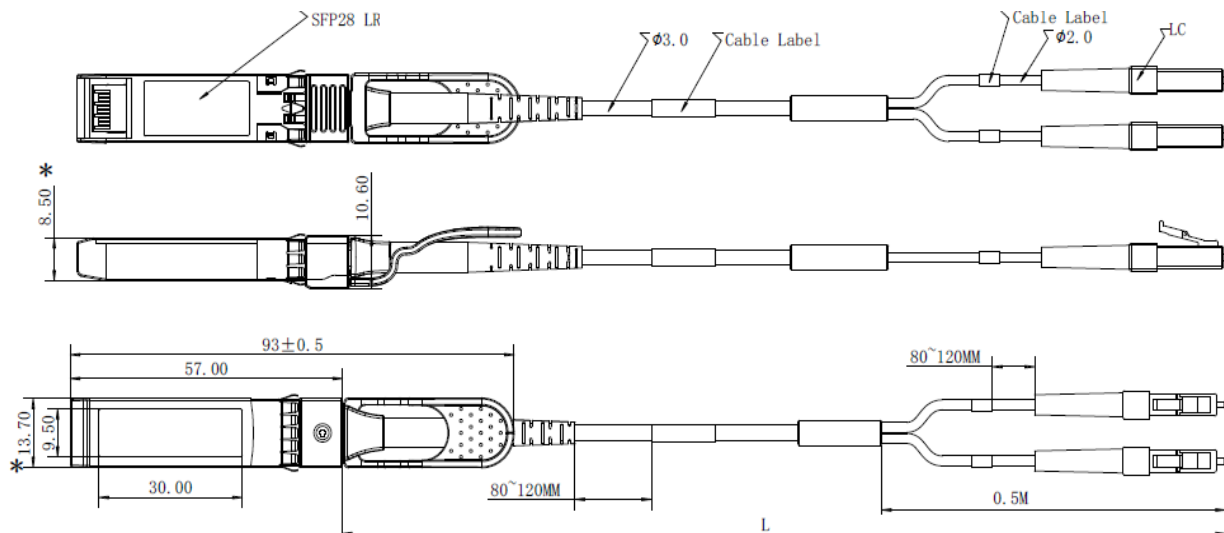
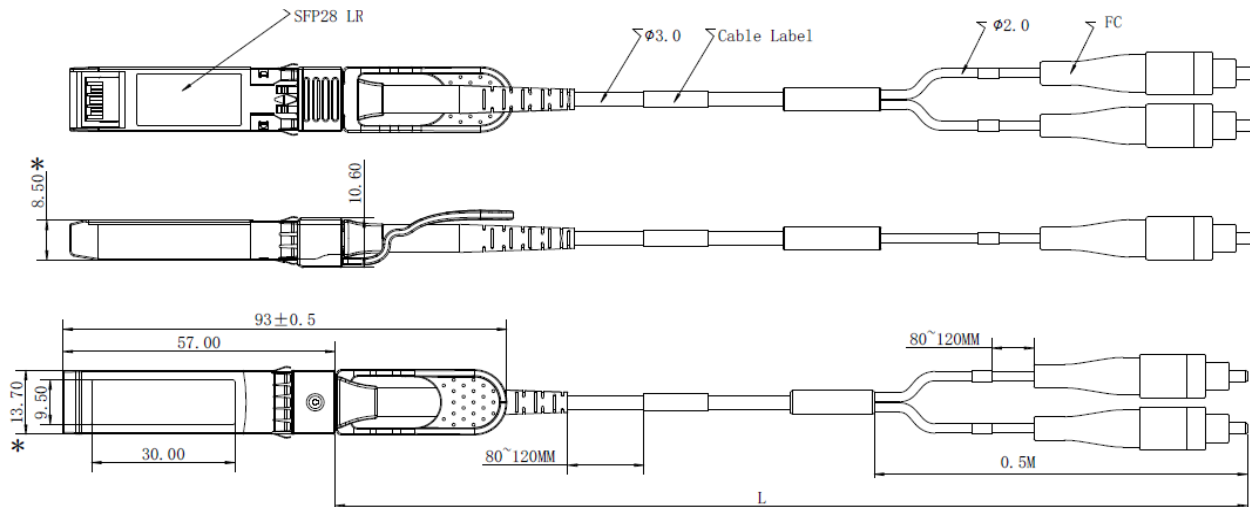
| Pin | Logic     | Symbol   | Description                                                 |
|-----|-----------|----------|-------------------------------------------------------------|
| 1   |           | VeeT     | Module Transmitter Ground                                   |
| 2   | LVTTL-O   | Tx_Fault | Module Transmitter Fault                                    |
| 3   | LVTTL-I   | Tx_DIS   | Transmitter Disable; Active High Disable Transmitter Output |
| 4   | LVTTL-I/O | SDA      | 2-Wire Serial Interface Data                                |
| 5   | LVTTL-I/O | SCL      | 2-Wire Serial Interface Clock                               |
| 6   |           | Mod_ABS  | Module Absent, connected to VeeT or VeeR in the module      |
| 7   | LVTTL-I   | RS0      | Rate Select0, optionally controls SFP+ module receiver      |
| 8   | LVTTL-O   | RX_LOS   | Receiver Loss of Signal Indication                          |
| 9   | LVTTL-I   | RS1      | Rate Select1, optionally controls SFP+ module transmitter   |
| 10  |           | VeeR     | Module Receiver Ground                                      |
| 11  |           | VeeR     | Module Receiver Ground                                      |
| 12  | CML-O     | RD-      | Receiver Inverted Data Output                               |
| 13  | CML-O     | RD+      | Receiver Non-Inverted Data Output                           |
| 14  |           | VeeR     | Module Receiver Ground                                      |
| 15  |           | VccR     | Module Receiver 3.3V Supply                                 |
| 16  |           | VccT     | Module Transmitter 3.3V Supply                              |
| 17  |           | VeeT     | Module Transmitter Ground                                   |
| 18  | CML-I     | TD+      | Transmitter Non-Inverted Data Input                         |
| 19  | CML-I     | TD-      | Transmitter Inverted Data Input                             |
| 20  |           | VeeT     | Module Transmitter Ground                                   |

## Recommended Interface Circuit





### Mechanical Dimensions(FC/LC)





## Regulatory Compliance

These optical transceivers are classified as Class 1 Laser Products and comply with the following laser safety standards:

| Feature                  | Standard                                                                                                 |
|--------------------------|----------------------------------------------------------------------------------------------------------|
| Laser Safety             | IEC 60825-1:2014 (3rd Edition)<br>IEC 60825-2:2004/AMD2:2010<br>EN 60825-1:2014<br>EN 60825-2:2004+A1+A2 |
| Electrical Safety        | EN 62368-1: 2014<br>IEC 62368-1:2014<br>UL 62368-1:2014                                                  |
| Environmental protection | Directive 2011/65/EU with amendment(EU)2015/863                                                          |
| CE EMC                   | EN55032:2015<br>EN55035:2017<br>EN61000-3-2:2014<br>EN61000-3-3:2013                                     |
| FCC                      | FCC Part 15, Subpart B<br>ANSI C63.4-2014                                                                |

## References

- SFP28 MSA
- Ethernet IEEE802.3cc
- Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011.



## Laser Safety Warning

Caution: Use of optical instruments with this product will increase eye hazard. Do not view the laser beam directly with optical instruments or naked eyes.

## Disclaimer

Images are for illustrative purposes only and may not accurately represent the actual product. Specifications and appearances are subject to change without prior notice.

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