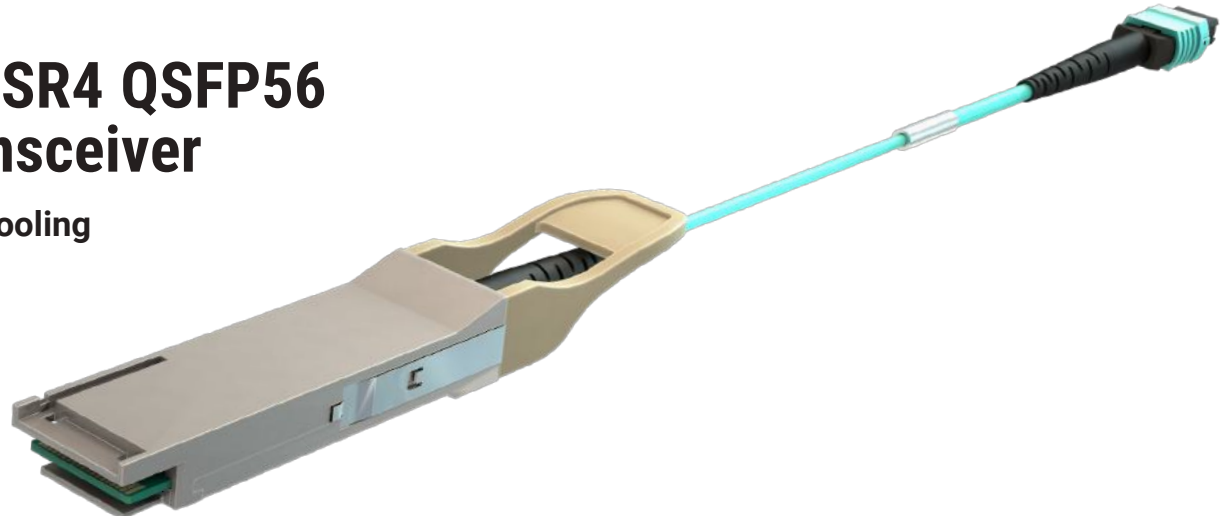




200GBASE-SR4 QSFP56 Optical Transceiver

Module for liquid cooling



Key Feature

- Hot-pluggable QSFP56 form factor
- Built-in 200G PAM4 DSP
- Supports 212.5Gb/s aggregate bit rates
- Supports 103.125Gb/s aggregate bit rates if required^{Note1}
- Low power dissipation <5W
- RoHS-6 compliant (lead-free)
- Operating case temperature: Commercial (0°C to +70°C)
- Single 3.3V power supply
- Maximum link length of 70m on OM3 MMF and 100m on OM4& OM5 MMF
- 4 channels 850nm VCSEL array and PIN PD array
- Single male MPO12 pigtail
- Built-in digital diagnostic functionality and CMIS V4.0 compliant

Applications

- IEEE 802.3cd 200GBASE-SR4 Ethernet (PAM4)
- IEEE 802.3bm 100GBASE-SR4 Ethernet (NRZ)^{Note1}

Especially designed for liquid immersion cooling environments

Note1:

Contact Support for more details

Standard Compliance

- QSFP MSA
- CMIS V4.0

Ordering Information - 200GBASE-SR4 QSFP56 Optical Transceiver

Part No.	Data Rate	Distance	Wavelength	Media	Connector	Temp.
LIQM-NKSxxxC	200G	~100m	850nm	MMF	MPO-12 APC	C

Product Description

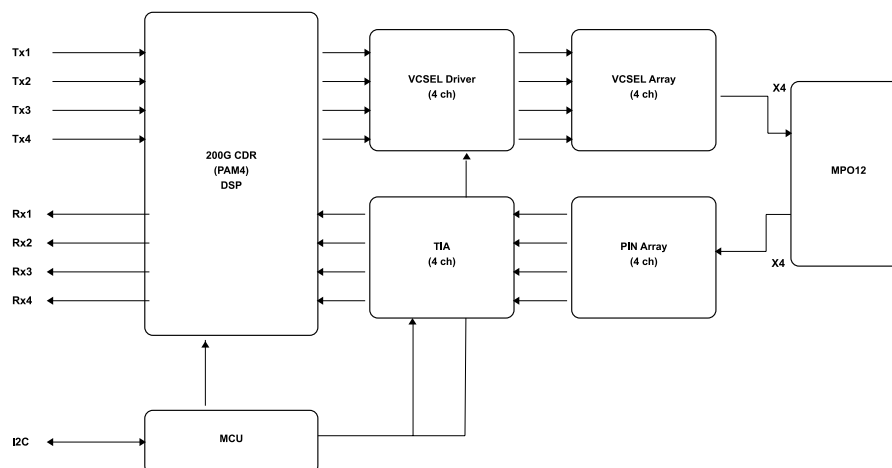
The 200G QSFP56 Optical Transceiver is designed for 200 Gigabit Ethernet links over OM3, OM4, and OM5 multimode fiber, with optimized performance in liquid immersion cooling environments.

The module complies with the QSFP56 MSA, IEEE 802.3cd 200GBASE-SR4, and CMIS Rev. 4.0 specifications. Digital diagnostic monitoring (DDM) functions are available through the I²C management interface as defined by CMIS.

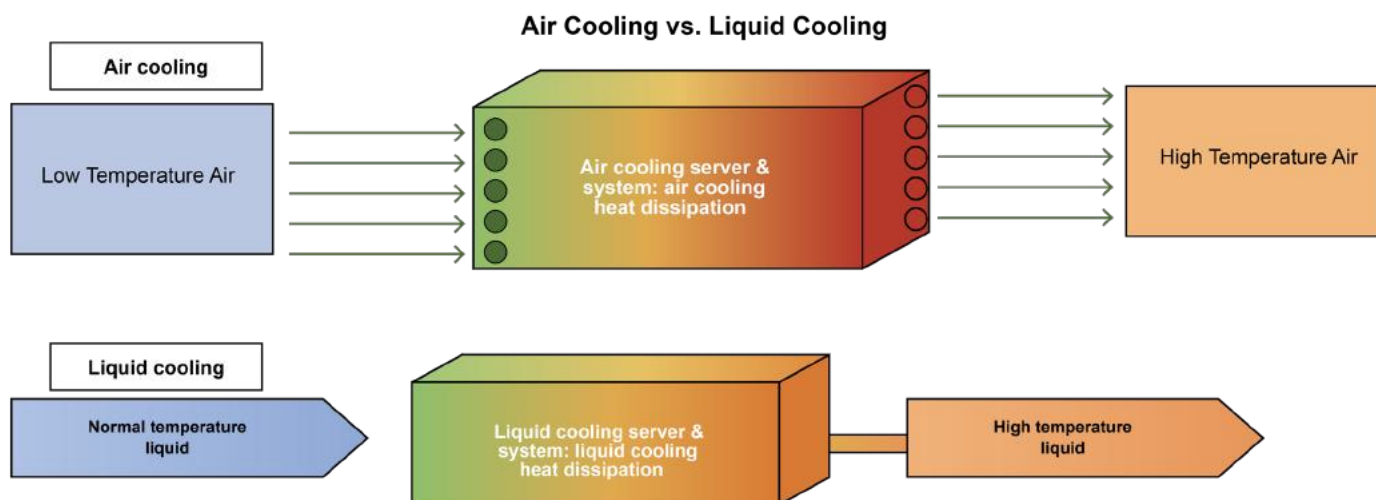
The transceiver integrates four transmit and four receive lanes, each operating at 53.125 Gb/s, providing an aggregate data rate of 200 Gb/s.

The optical interface utilizes a male MPO-12 optical pigtail. The internal optical assembly is sealed using a specialized protection technology designed to prevent dielectric cooling fluid ingress, ensuring reliable operation in liquid immersion cooling applications.

Module Block Diagram



Liquid cooling advantage



Liquid Immersion Cooling Applications

As data traffic continues to grow and the heat generated by high-performance processors and AI accelerators increases, conventional air-cooling solutions are reaching their practical limits. Liquid cooling technologies provide a more efficient method of heat removal by using dielectric fluids with high thermal capacity, significantly improving cooling efficiency and reducing overall data center power consumption.

This optical transceiver is specifically designed for operation in liquid immersion cooling environments, providing reliable operation when fully immersed in dielectric immersion fluids at depths of up to 10 meters. It is ideally suited for liquid-cooled servers, switches, and high-performance computing systems. The module is compatible with a wide range of dielectric immersion fluids, including fluorinated fluids and mineral oils, ensuring long-term reliability and stable optical performance in demanding immersion cooling applications.



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{cc}	-0.3	3.6	V
Input Voltage	V _{in}	-0.3	V _{cc} +0.3	V
Storage Temperature	T _{st}	-20	85	°C
Case Operating Temperature	T _{op}	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V _{cc}	3.13	3.3	3.47	V
Operating Case temperature	T _{ca}	0		70	°C
Baud Rate per Lane (PAM4)	fd		53.125		GBaud/s
Humidity	Rh	5		85	%
Power Dissipation	P _m		4.1	4.5	W
Fiber Bend Radius	R _b	3			cm
Liquid immersion depth				10	m

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Z _{in}	90	100	110	ohm
Differential Output impedance	Z _{out}	90	100	110	ohm
Differential input voltage amplitude	ΔV _{in}	300		1000	mVp-p
Differential output voltage	ΔV _{out}	300		900	mVp-p
Bit Error Rate	BER			2.4E-4	
Input Logic Level High	V _{IH}	2.0		V _{cc}	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	V _{cc} -0.5		V _{cc}	V
Output Logic Level Low	V _{OL}	0		0.4	V

Notes:

Compliant with 200GBASE-SR4 electrical specification in IEEE802.3cd standard


Optical Characteristics

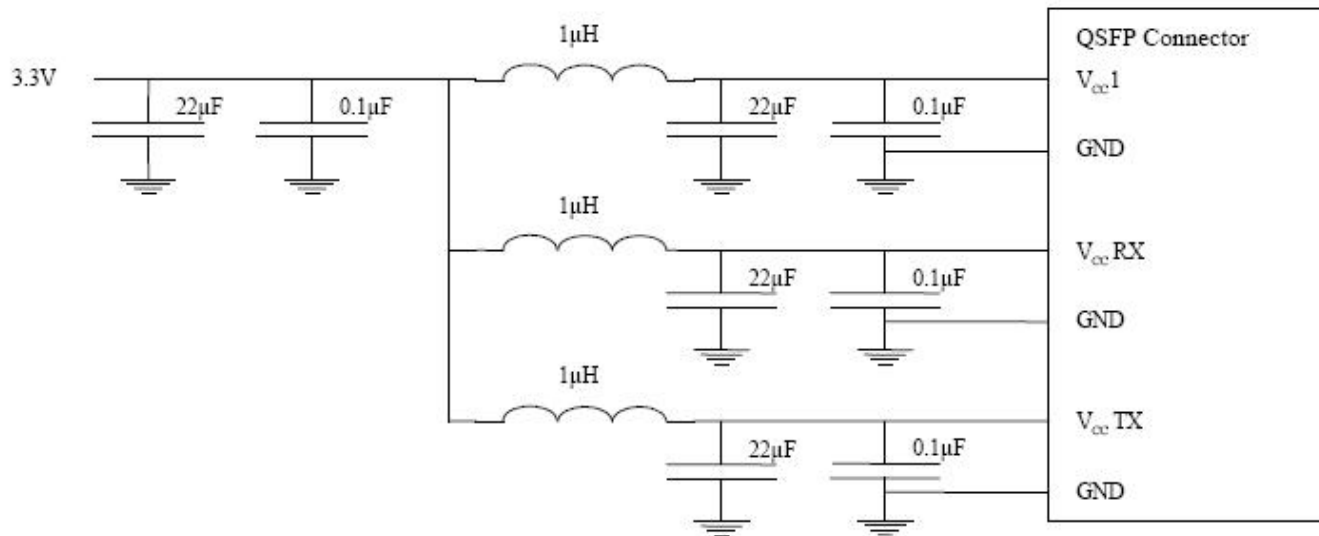
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ_c	840	850	860	nm	
RMS spectral width	$\Delta\lambda$			0.6	nm	
Average launch power, each lane	P _{out}	-6.5		4	dBm	
Optical Modulation Amplitude (each lane)	OMA	-4.5		3	dBm	
Transmitter and dispersion eye closure, each lane	TDEC			4.5	dB	
Outer Extinction Ratio	ER	3			dB	
Optical Return Loss Tolerance	ORLT			12	dB	
Receiver						
Centre Wavelength	λ_c	840	850	860	nm	
Damage threshold	R _{dam}			4	dBm	
Average Receive Power (each lane)	P _{in}	-7.9		4	dBm	
Receiver Power (OMA _{outer}) (each lane)	OMA _{out}			3	dBm	
Receiver reflectance	P _{ref}			-12	dB	
Stressed Receiver Sensitivity (OMA _{outer}) (each lane)	Sens			-3	dBm	

Notes:

Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

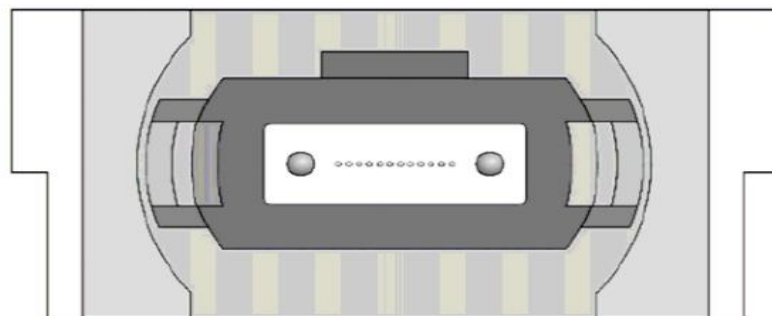


Power Supply Filtering



Optical Interface Lanes and Assignment

The optical interface port is amale MPO-12 APC pigtail available in custom lengths. The four fiber positions on the left as shown in Figure 4, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1).



Transmit Channels: 1 2 3 4
 Unused positions: x x x x
 Receive Channels: 4 3 2 1

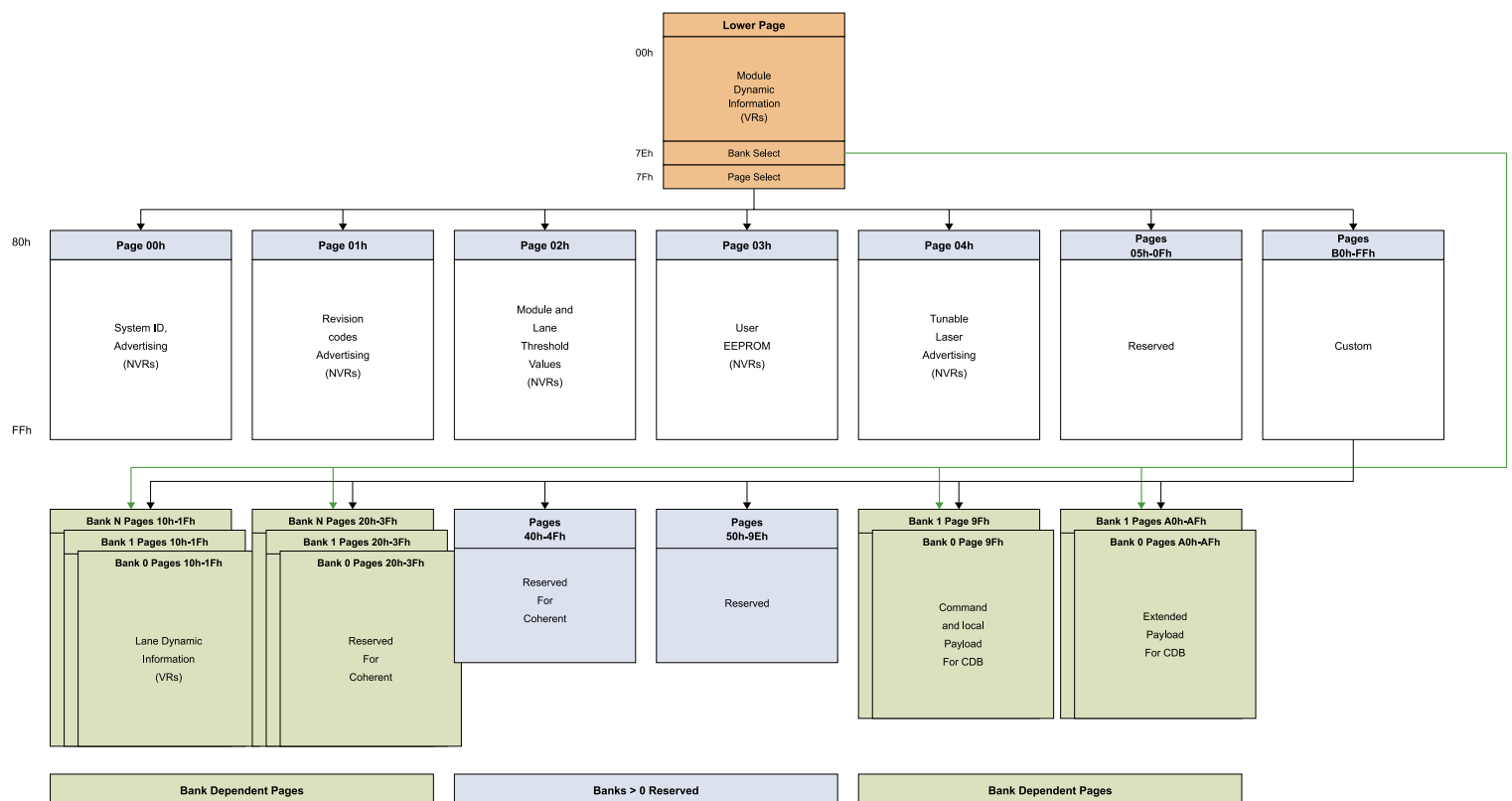
DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics functions are available via the I2C interface as specified by CMIS V4.0. The CMIS management memory is shown in Figure below.

Due to eight-bit addresses, the management memory is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h ~ FFh).

The addressing structure of the additional internal management memory is shown in the next figure. The management memory is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

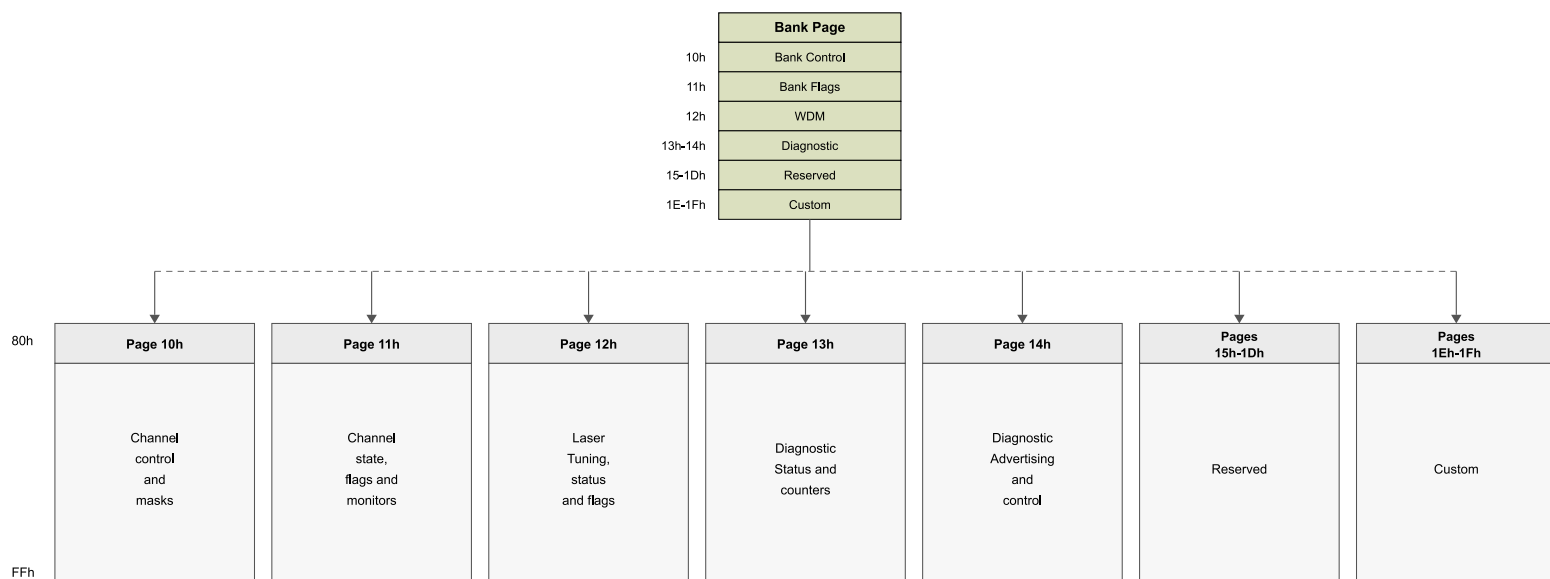
This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory(e.g. Flags and Monitors). Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page.



The CMIS memory structure also provides address expansion by adding additional upper pages as needed. Upper pages 00-02 all contain static, non-volatile advertising registers. Upper page 01 provides revision codes and advertising registers that indicate the capabilities of the module. Upper page 02 provides thresholds for monitored functions. Upper page 03 provides a user read/write space.



The lower page, upper pages 00h-03h and bank 0 page 10h-11h are supported in our module.



Additional Supported Bank Page Memory Map

The Lower Memory– Page 00h

The Lower Memory consists of the lower 128 bytes of the 256 byte two-wire serial bus addressable space. The Lower Page is used to access a variety of module level measurements, diagnostic functions and control functions, as well as to select which of the various Upper Pages in the structured memory map are accessed by byte addresses greater or equal than 128.

Address	Size	Subject Area	Description
0–3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4–7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page



The Upper Memory – Page 00h Memory Overview

Upper page 00h contains static read-only module identification information.

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

The Upper Memory – Page 01h(Advertising)

Upper page 01h contains advertising fields that define properties that are unique to active modules and cable assemblies.

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Memory Pages and Durations advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-166	4	CDB support advertising	
167-168	2	Additional Durations advertising	
169-175	7	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
223-250	28	Extended Module Host-Media Interface Advertising options	
251-254	4	Reserved	
255	1	Checksum	Checksum of bytes 130-254 ¹



The Upper Memory – Page 02h (Module and Lane Thresholds)

Upper Page 02h contains the module-defined thresholds for module-level and lane-specific monitors. The presence of Page 02h is advertised in bit 7 in Page 00h byte 2.

Byte	Size (bytes)	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	
230-254	25	Custom	
255	1	Checksum	Covers bytes 128-254

The Upper Memory – Page 10h (Lane and Data Path Control)

The upper memory map page 10h is a banked page that contains lane dynamic control bytes. The presence of Page 10h is advertised in bit 7 in Page 00h byte 2.

Byte	Size (bytes)	Name	Description
128	1	DataPathDeinit	Data Pathcontrol bits for each lane, controls Data Path State machine
129-142	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
143-177	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
178-212	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
213-231	19	Lane-Specific Flag Masks	
232-239	8	Reserved	
240-255	16	Custom	

The Upper Memory – Page 11h (Lane Status)

The upper memory map page 11h is a banked page that contains lane dynamic status bytes. The presence of Page 11h is conditional on the state of bit 7 in Page 00h byte 2. All fields on Page 11h are read-only.

Byte	Size (bytes)	Name	Description
128-131	4	Data Path State indicators	
132-133	2	Reserved	
134-152	19	Lane-specific flags	
153	1	Reserved	
154-201	48	Lane-specific monitors	
202-205	4	Configuration Error Codes	Indicates validity of select Application codes
206-234	29	Active Control Set	
235-239	5	Reserved	
240-255	16	Host Electrical to Module Media Lane Mapping	Indicates the mapping of Host Electrical lanes to Module Media lanes



QSFP56 PIN Function Definitions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-wire serial interface clock
12	LVC MOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Present
28	LVTTL-O	IntL/RxLOSL	Interrupt/optional RxLOS
29		Vcc Tx	+3.3 V Power supply transmitter
30		Vcc1	+3.3 V Power Supply



31	LVTTL-I	LPMode/TxDis	Low Power Mode/optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground

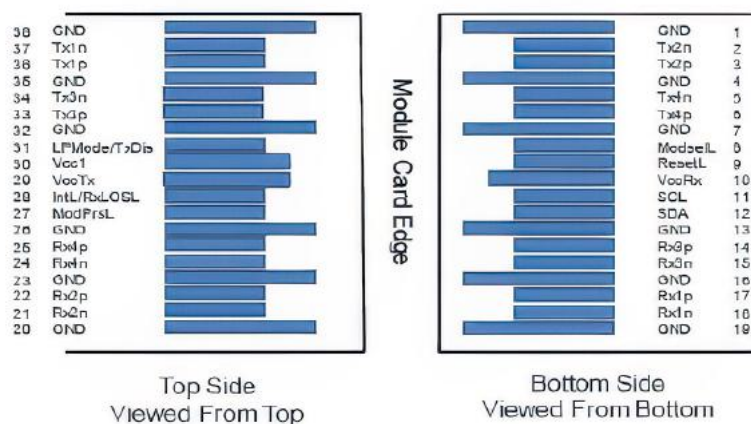
Note:

Module circuit ground is isolated from module chassis ground within the module.

Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

QSFP56 Electrical Pad Layout

For detail mechanical information, please refer to the related document of QSFP MSA.



**ModSelL Pin**

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMODE_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length ($t_{\text{Reset_init}}$) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMODE Pin

QSFP56 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

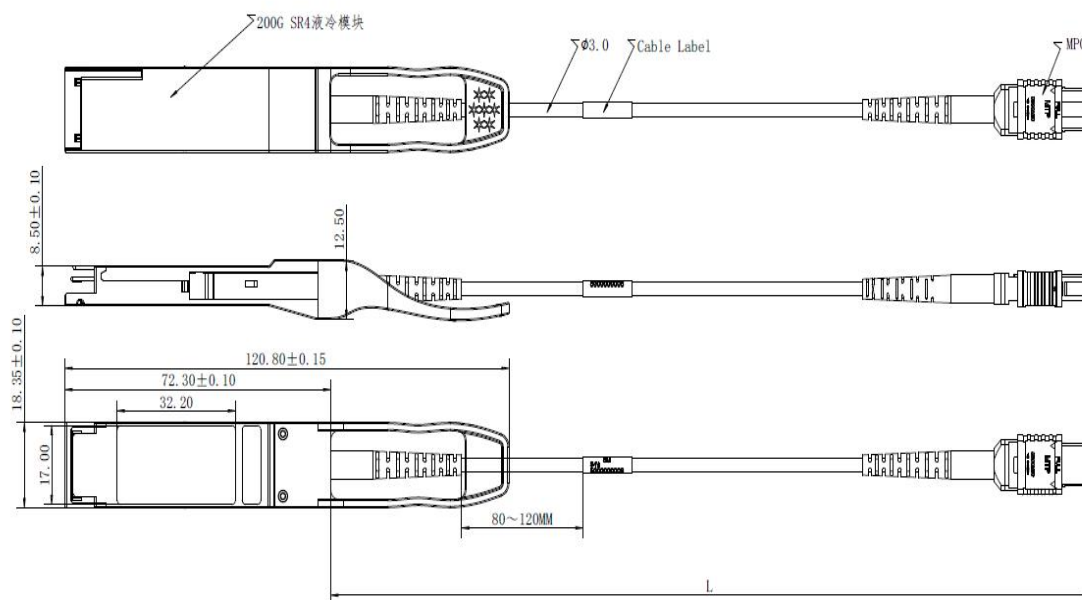
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.



Mechanical Dimensions(mm)



Regulatory Compliance

These optical transceivers are classified as Class 1 Laser Products and comply with the following laser safety standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1:2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032:2015 EN55035:2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014



Laser Safety Warning

Caution: Use of optical instruments with this product will increase eye hazard. Do not view the laser beam directly with optical instruments or naked eyes.

Disclaimer

Images are for illustrative purposes only and may not accurately represent the actual product. Specifications and appearances are subject to change without prior notice.

The information provided in this datasheet is subject to change without notice. Lumulus Technologies assumes no responsibility for any errors or omissions. Performance may vary depending on application and operating conditions. Product specifications are provided for reference only and do not constitute a warranty.

For assistance and more information, please contact your sales representative or write to sales@lumulus.com

Lumulus Technologies, Inc. USA

Headquarters

9685 Via Excelencia Suite 106
 San Diego, CA 92126
 USA

 (+1) 858-397-2228

 www.lumulus.com

Lumulus Technologies, Inc. Thailand

Production site

Sri Ayutthagya - Thailand