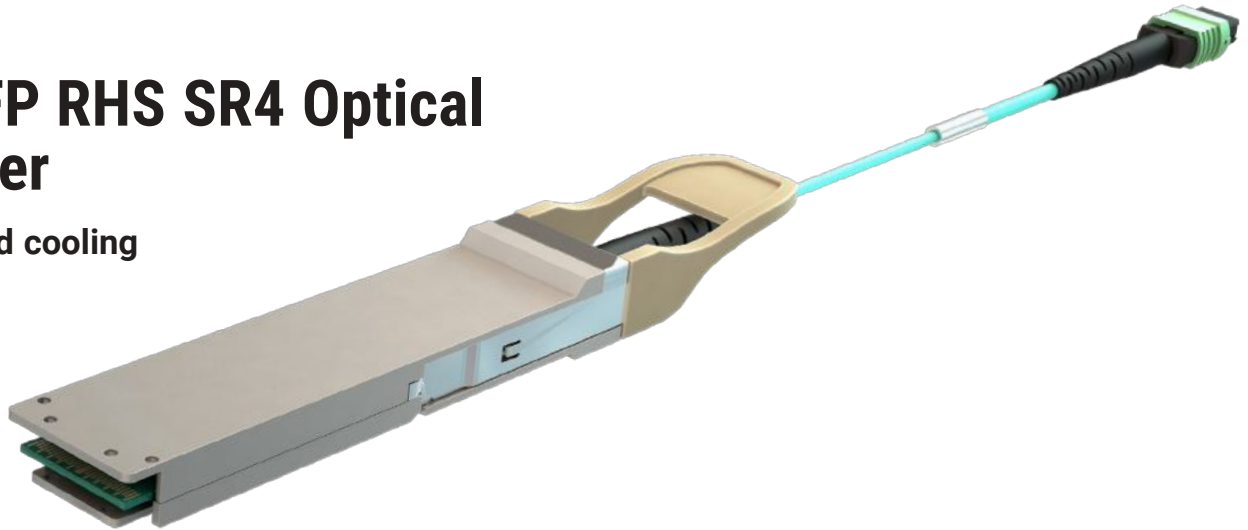




400G OSFP RHS SR4 Optical Transceiver

Module for liquid cooling



Key Feature

- 4 channels full-duplex transceiver modules
- Transmission data rate up to 106.25G per channel
- 4x106.25Gbps PAM4 transmitter and PAM4 receiver
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Power consumption <8W
- Hot-Pluggable OSFP RHS form factor and Compliant with CMIS
- Up to 60 m over OM3 MMF
- Up to 100 m over OM4 MMF (with FEC)
- Male MPO12 APC pigtail
- Built-in digital diagnostic functions
- Operating case temperature: Commercial (0°C to +70°C)
- 3.3V power supply voltage
- RoHS compliant(lead free)

Applications

- IEEE 802.3db 400GBASE-SR4 Ethernet (PAM4)
- The transceiver is designed for Ethernet, Telecom and Infiniband use cases.
- Especially designed for liquid immersion cooling environments

Ordering Information - 400G OSFP RHS SR4 liquid immersion transceiver

Part No.	Data Rate	Distance	Wavelength	Media	Connector	Temp.
LIRM-PMSxxxC	400G	~100m	850nm	MMF	MPO-12 APC	C

Product Description

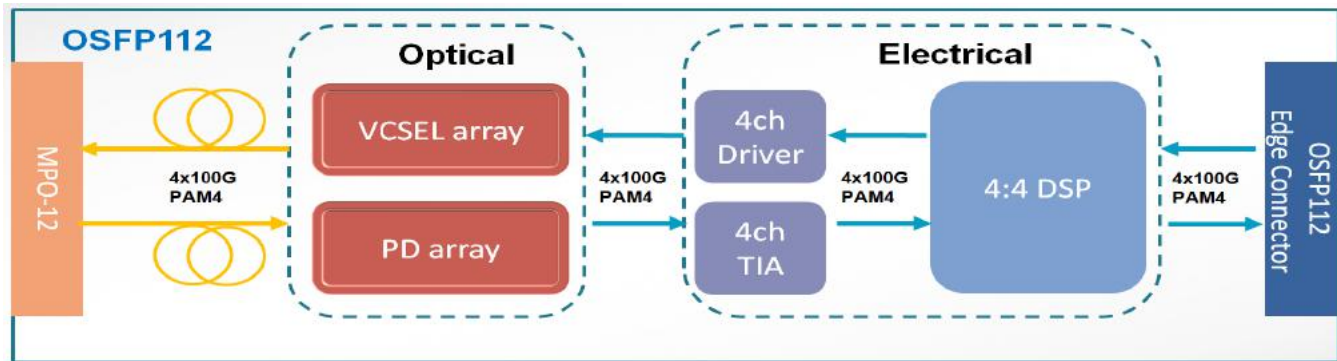
The module is a high-performance optical transceiver designed for short-range, multi-lane data communication and interconnect applications in liquid immersion environments.

It integrates four transmit and four receive lanes, each operating at 53.125 Gb/s. With FEC enabled, each lane supports data rates of up to 106.25 Gb/s, providing transmission distances of up to 60 m over OM3 multimode fiber and up to 100 m over OM4 multimode fiber.

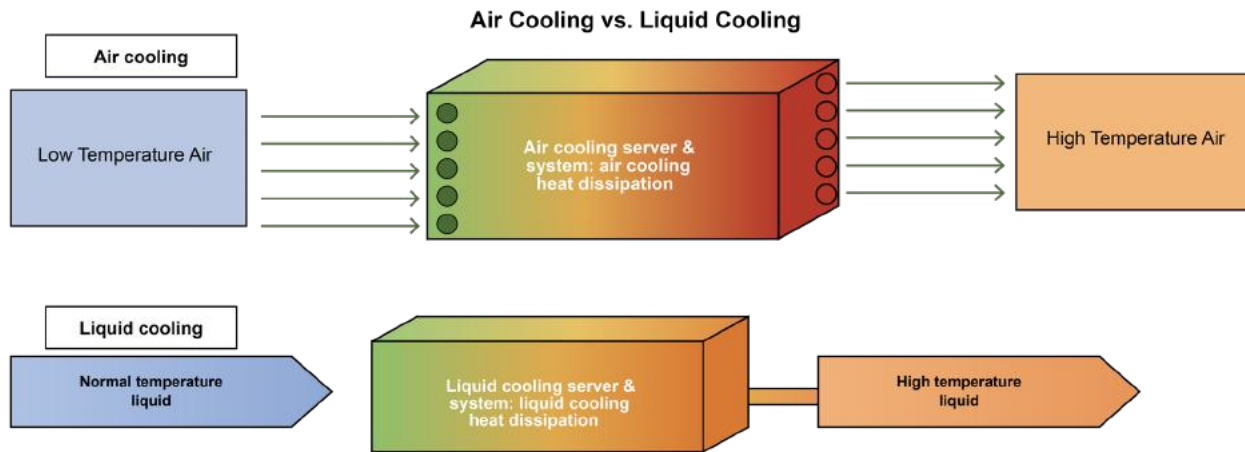
Designed for multimode fiber systems operating at a nominal wavelength of 850 nm, the module features a male MPO-12 APC optical pigtail interface. It incorporates advanced VCSEL technology and a high reliability optical design to deliver long operational life, consistent performance, and dependable operation in demanding data center and liquid immersion cooling environments.



Module Block Diagram



Liquid cooling advantage



Liquid Immersion Cooling Applications

As data traffic continues to grow and the heat generated by high-performance processors and AI accelerators increases, conventional air-cooling solutions are reaching their practical limits. Liquid cooling technologies provide a more efficient method of heat removal by using dielectric fluids with high thermal capacity, significantly improving cooling efficiency and reducing overall data center power consumption.

This optical transceiver is specifically designed for operation in liquid immersion cooling environments, providing reliable operation when fully immersed in dielectric cooling fluids at depths of up to 10 meters. It is ideally suited for liquid-cooled servers, switches, and high-performance computing systems. The module is compatible with a wide range of dielectric cooling fluids, including fluorinated fluids and mineral oils, ensuring long-term reliability and stable optical performance in demanding immersion cooling applications.



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane			106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		7.5	8	W
Fiber Bend Radius	Rb	3			cm
Liquid immersion depth				10	m

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔV_{in}	400		900	mVp-p
Differential output voltage	ΔV_{out}			850	mVp-p
Bit Error Rate	BER			2.4E-4	
Input Logic Level High	VIH	2.0		Vcc	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	Vcc-0.5		Vcc	V
Output Logic Level Low	VOL	0		0.4	V
Input Logic Level High	VIH	2.0		Vcc	V

Notes:

1. BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.



Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ_c	844	850	863	nm	
RMS spectral width	$\Delta\lambda$			0.6	nm	
Average launch power, each lane	P _{out}	-4.6		4	dBm	
Optical Modulation Amplitude (OMA _{outer}), each lane	OMA	-2.6		3.5	dBm	
Transmitter and dispersion eye closure for PAM4(TDECQ),each lane	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5			dB	
Average launch power of OFF transmitter, each lane				-30	dB	
Receiver						
Centre Wavelength	λ_c	842	850	948	nm	
Receiver Sensitivity (OMA _{outer})	RX _{sen}			max (-4.6,TECQ 6.4)	dBm	1
Stressed Receiver Sensitivity (OMA _{outer})	SRS			-2	dBm	2
Maximum Average power at receiver , each lane input, each lane				4	dBm	
Minimum Average power at receiver , each lane		-6.4			dBm	
Receiver Reflectance				-15	dB	
LOS Assert	LOSA	-15		-8.5	dBm	
LOS De-Assert	LOSD			-6.5	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

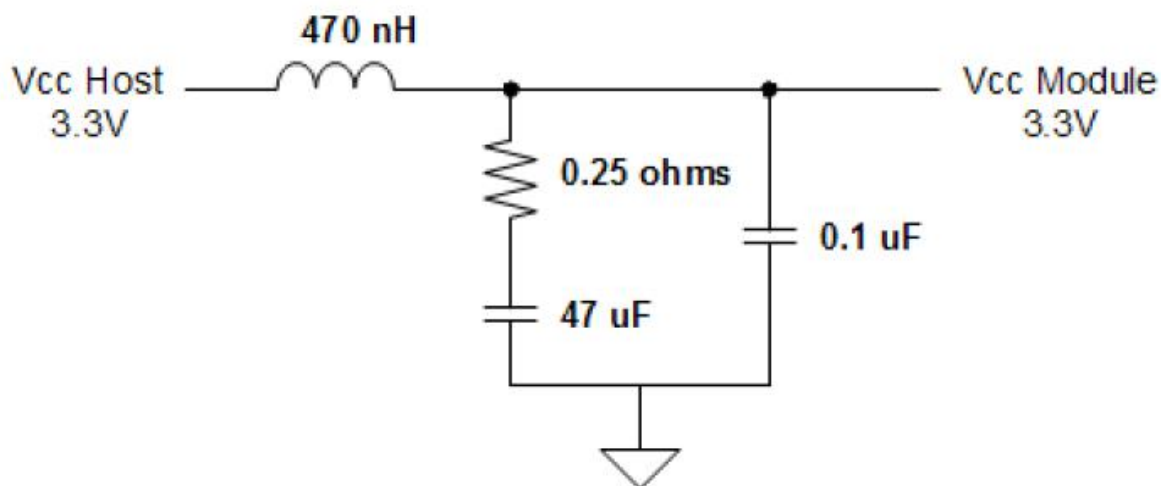
1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	°C	Over operating temp
Supply voltage monitor absolute error	DMI_VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

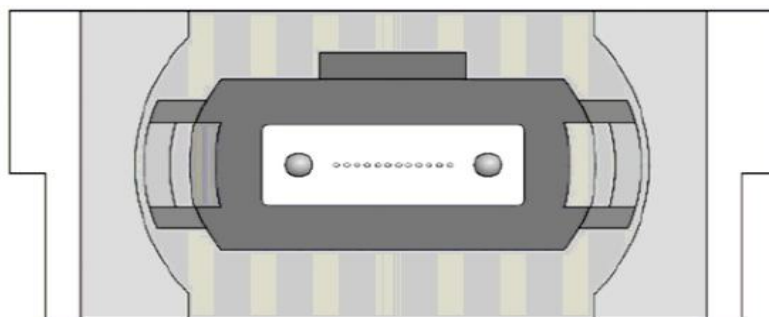


Power Supply Filtering



Optical Interface Lanes and Assignment

The optical interface port is male MPO-12 APC pigtail



Transmit Channels: 1 2 3 4
 Unused positions: x x x x
 Receive Channels: 4 3 2 1



DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all OSFP products. A 2-wire serial interface provides communication between the host and module.

Memory Structure and Mapping

The module management memory directly accessible by the host is limited to 256 bytes and is divided into two regions: Lower Memory (addresses 00h to 7Fh) and Upper Memory (addresses 80h to FFh).

Since 256 bytes are insufficient for all but the simplest modules, the management interface supports an extended memory architecture based on 128-byte pages. Through a dynamic page mapping mechanism, any available 128-byte page within the internal management memory can be mapped into the host-accessible Upper Memory address space.

The internal management memory is organized as a permanently accessible 128-byte Lower Memory region and multiple 128-byte Upper Memory pages, with only one page visible to the host at any given time. For page groups containing multiple instances, an additional bank selection mechanism provides access to pages sharing the same page number.

This architecture provides a flat 256-byte memory map for passive copper modules while ensuring immediate access to time-critical information stored in Lower Memory, such as status flags and monitoring data. Less time-sensitive information, including serial identification data and threshold settings, can be accessed by selecting the appropriate page through the Page Select function.

For more advanced modules requiring additional management memory, the host dynamically maps the required pages into the Upper Memory address space as needed.

The management memory architecture supports eight electrical lanes while optimizing overall memory usage. A single management interface is used, with paging implemented to provide efficient access to both time-critical monitoring information and extended management data.

Supported Pages

A basic 256-byte Management Memory Map is mandatory for all CMIS-compliant modules. Additional memory areas are available only for paged memory modules or when explicitly supported and advertised by the module. Refer to the CMIS Specification Rev. 4.0 for detailed information on supported management memory spaces.

Support for Lower Memory and Page 00h is mandatory for all modules, including passive copper cable assemblies. These memory regions are therefore always implemented. For paged memory modules, support for Pages 01h, 02h, and Bank 0 of Pages 10h and 11h is also mandatory.

Bank 0 of Pages 10h through 1Fh provides lane-specific registers for the first eight electrical lanes. Each additional bank extends support to the next group of eight lanes. Depending on the page definition, the allocation of information across banks may vary and is not necessarily organized in groups of eight lanes.

The paged memory architecture allows the management address space to be expanded by implementing additional pages and, where required, additional page banks to support more advanced module functionality.



Memory Map Structure

This memory structure provides a scalable addressing scheme, allowing the address space to be expanded through the implementation of additional pages and banks as required by specific module types and future feature enhancements.

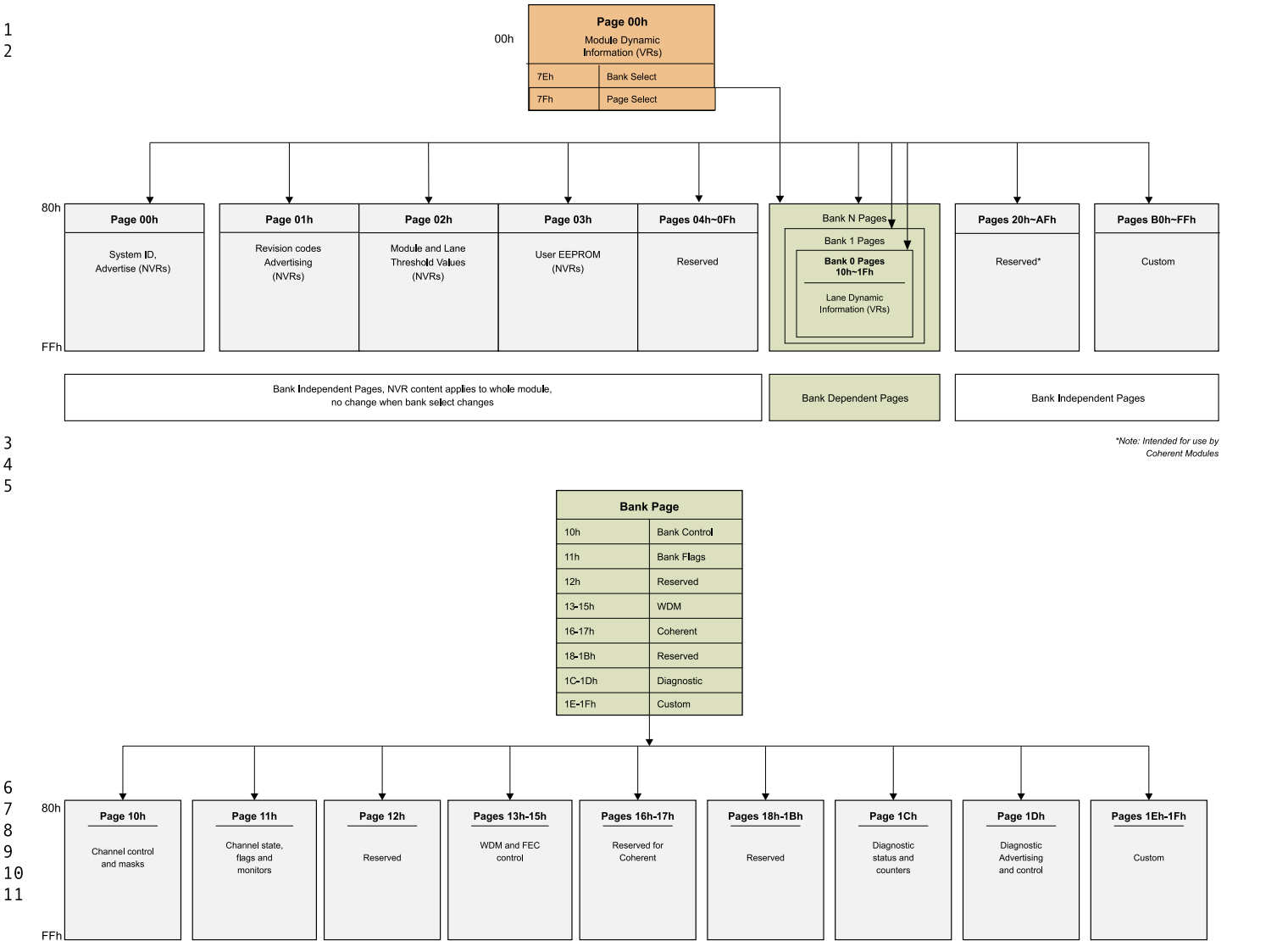
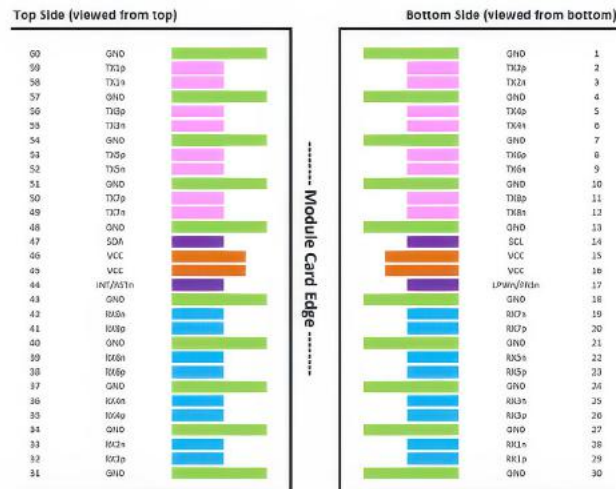


Figure 11: CMIS Module Memory Map



OSFP Electrical Pad Layout

For detail mechanical information, please refer to the related document of OSFP MSA.



OSFP Control Pins

Name	Function	Description
LPWn/PRSn	Input/output	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.
INT/RSTn	Input,/output	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in the OSFP Specification.
SCL	BiDir	2wire serial clock signal. Requires pullup resistor to 3.3V on host.
SDA	Bidir	2wire serial data signal. Requires pullup resistor to 3.3V on host.



OSFP PIN Function Definitions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2p	Transmitter Data Non-Inverted
3	CML-I	Tx2n	Transmitter Data Inverted
4		GND	Ground
5	CML-I	Tx4p	Transmitter Data Non-Inverted
6	CML-I	Tx4n	Transmitter Data Inverted
7		GND	Ground
8	CML-I	Tx6p	Transmitter Data Non-Inverted
9	CML-I	Tx6n	Transmitter Data Inverted
10		GND	Ground
11	CML-I	Tx6p	Transmitter Data Non-Inverted
12	CML-I	Tx6n	Transmitter Data Inverted
13		GND	Ground
14	LVCMOS-I/O	SCL	2-wire serial interface clock
15		VCC	+3.3V Power
16		VCC	+3.3V Power
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present
18		GND	Ground
19	CML-O	Rx7n	Receiver Data Inverted
20	CML-O	Rx7p	Receiver Data Non-Inverted
21		GND	Ground
22	CML-O	Rx5n	Receiver Data Inverted
23	CML-O	Rx5p	Receiver Data Non-Inverted



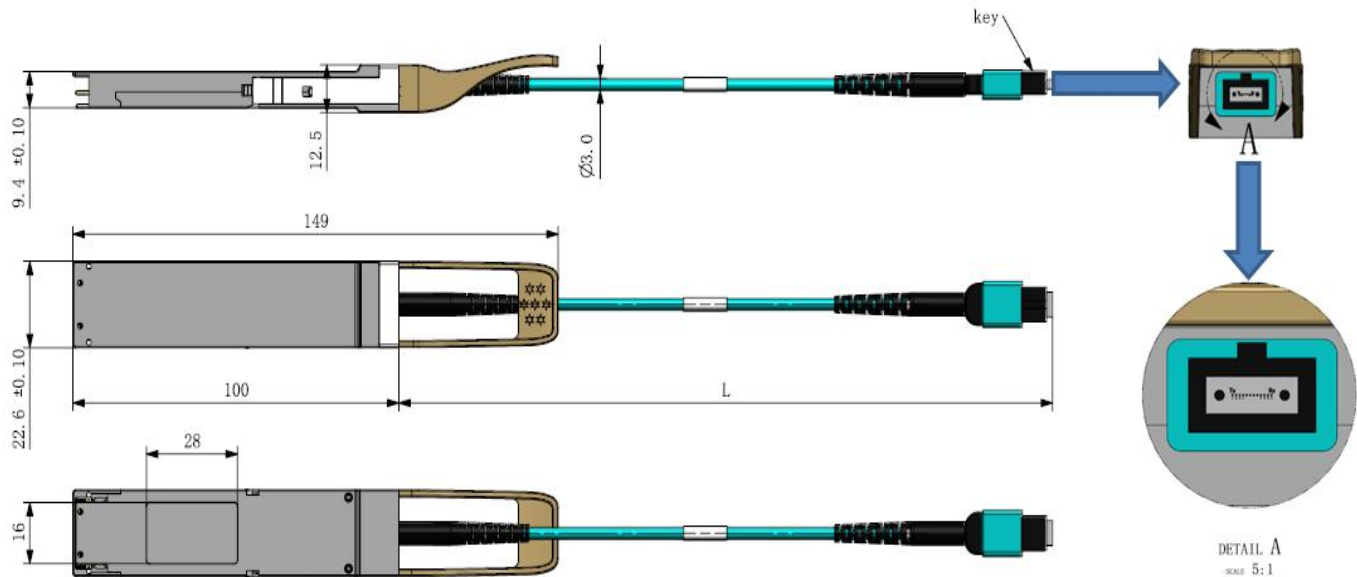
24		GND	Ground
25	CML-O	Rx3n	Receiver Data Inverted
26	CML-O	Rx3p	Receiver Data Non-Inverted
27		GND	Ground
28	CML-O	Rx1n	Receiver Data Inverted
29	CML-O	Rx1p	Receiver Data Non-Inverted
30		GND	Ground
31		GND	Ground
32	CML-O	Rx2p	Receiver Data Non-Inverted
33	CML-O	Rx2n	Receiver Data Inverted
34		GND	Ground
35	CML-O	Rx4p	Receiver Data Non-Inverted
36	CML-O	Rx4n	Receiver Data Inverted
37		GND	Ground
38	CML-O	Rx6p	Receiver Data Non-Inverted
39	CML-O	Rx6n	Receiver Data Inverted
40		GND	Ground
41	CML-O	Rx8p	Receiver Data Non-Inverted
42	CML-O	Rx8n	Receiver Data Inverted
43		GND	Ground
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset
45		VCC	+3.3V Power
46		VCC	+3.3V Power
47	LVC MOS-I/O	SDA	2-wire serial interface data
48		GND	Ground



49	CML-I	Tx7n	Transmitter Data Inverted
50	CML-I	Tx7p	Transmitter Data Non-Inverted
51		GND	Ground
52	CML-I	Tx5n	Transmitter Data Inverted
53	CML-I	Tx5p	Transmitter Data Non-Inverted
54		GND	Ground
55	CML-I	Tx3n	Transmitter Data Inverted
56	CML-I	Tx3p	Transmitter Data Non-Inverted
57		GND	Ground
58	CML-I	Tx1n	Transmitter Data Inverted
59	CML-I	Tx1p	Transmitter Data Non-Inverted
60		GND	Ground



Mechanical Dimensions(mm)



Regulatory Compliance

These optical transceivers are classified as Class 1 Laser Products and comply with the following laser safety standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1:2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032:2015 EN55035:2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014



Laser Safety Warning

Caution: Use of optical instruments with this product will increase eye hazard. Do not view the laser beam directly with optical instruments or naked eyes.

Disclaimer

Images are for illustrative purposes only and may not accurately represent the actual product. Specifications and appearances are subject to change without prior notice.

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