

SFP112 100G to SFP112 100G DAC



0.5~2.0M

PVC Black

Key Features

- Support 106.25G PAM4
- 100G to 100G Data Rate
- 3.3V Power Supply
- Hot Pluggable
- BER < 10⁻⁶ (pre FEC)
- BER < 10⁻¹⁵ (post FEC)
- Excellent SI performance
- RoHS Compliance

Applications

- Data center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices

Supported Standards

- SFP-DD MSA
- IEEE 802.3ck
- IEEE 802.3cd
- I2C for EEPROM
- CMIS 5.x



Ordering Information

LEPP-MM1xxxC SFP112 100G to SFP112 100G DAC – 0.5~2.0M

Ordering P/Ns	Description	Length	AWG	Cable	NOTE
LEPP-MM1xx5C	SFP112 100G to SFP112 100G DAC	0.5m	30 AWG	PVC Black	
LEPP-MM1x15C	SFP112 100G to SFP112 100G DAC	1.5m	28 AWG	PVC Black	
LEPP-MM1x20C	SFP112 100G to SFP112 100G DAC	2.0m	26 AWG	PVC Black	

xxx define DAC cable length

General Description

LEPP-MM1xxxC, SFP112 to SFP112 100G Direct Attached Cable Assembly is meticulously designed for application in the telecommunications and data center sectors. It helps carry 100Gb of traffic per cable in both directions. The cable adheres to the standardized SFP112 form factor and complies rigorously with MultiSource Agreement (MSA) specifications.

Absolute Maximum Ratings

Parameter	Unit	Min.	Max.	Notes
Supply Voltage	V	-0.3	3.6	
Data Input Voltage	V	-0.3	3.6	
Control Input Voltage	V	-0.3	3.6	
Operating Temperature	°C	0	70	
Storage Temperature	°C	-40	+85	
Relative Humidity (NonCondensing)	%	5	85	

Operational Specification

Parameter	Unit	Min	Typical	Max	Notes
Supply Voltage (Vcc)	V	3.135	3.3	3.465	Per End
Power Consumption	W			0.5	Per End
Operating Case Temperature	°C	0		70	
Operating Relative Humidity	%	0		85	
Modulation Format		112G PAM4			
Bit Rate	Gbps	100			

Electrical Characteristics

Parameter	Unit	Min	Typical	Max	Notes
Characteristic Impedance	ohm	90	100	110	
Time Propagation Delay (Informative)	ns			4.9	

SI performance

Parameter	Require	Reference
ILdd Insertion loss at 26.56 GHz	19.75 dB (Max.)	IEEE 802.3ck Section 162.11.2
ILdd Insertion loss at 26.56 GHz	11 dB (Min.)	IEEE 802.3ck Section 162.11.2
ERL Minimum cable assembly	>8.25 dB*.	IEEE 802.3ck Section 162.11.3
RLcd Differential mode to common mode return loss	0.01GHz – 40GHz Equation (162–20)	IEEE 802.3ck Section 162.11.4

ILcd	0.01GHz – 40GHz	IEEE 802.3ck Section
Differential mode to common mode insertion loss	Equation (162-21)	162.11.5
RLcc	0.01GHz – 40GHz	IEEE 802.3ck Section
Common mode to common mode return loss	Equation (162-22)	162.11.6
COM	3dB (Min.)	IEEE 802.3ck Section
		162.11.7

*Cable assemblies with a com greater than 4 dB are not required to meet minimum ERL

Cable Wiring

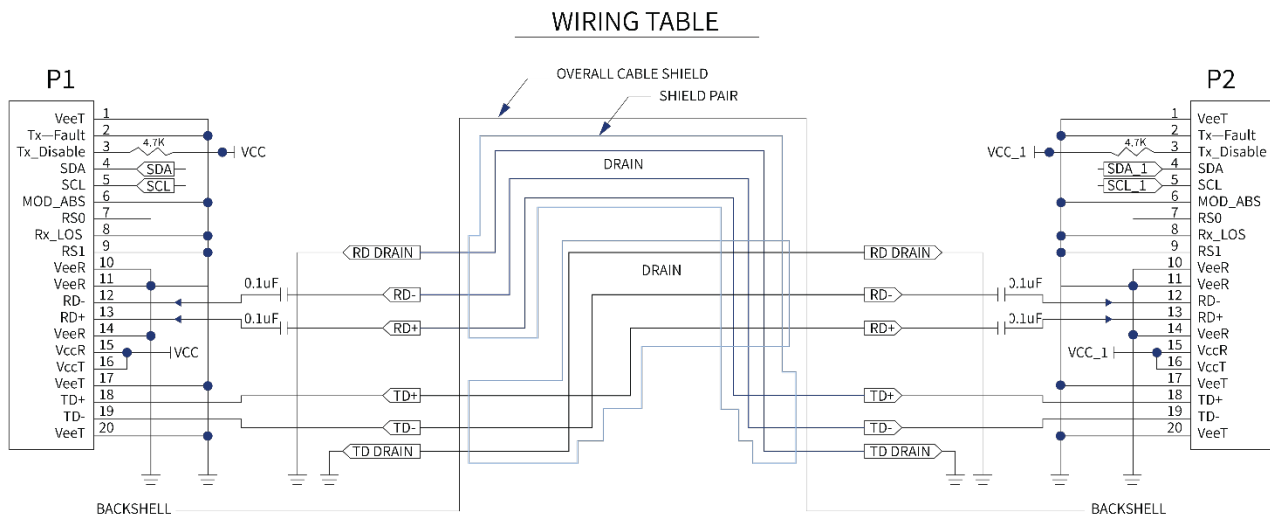
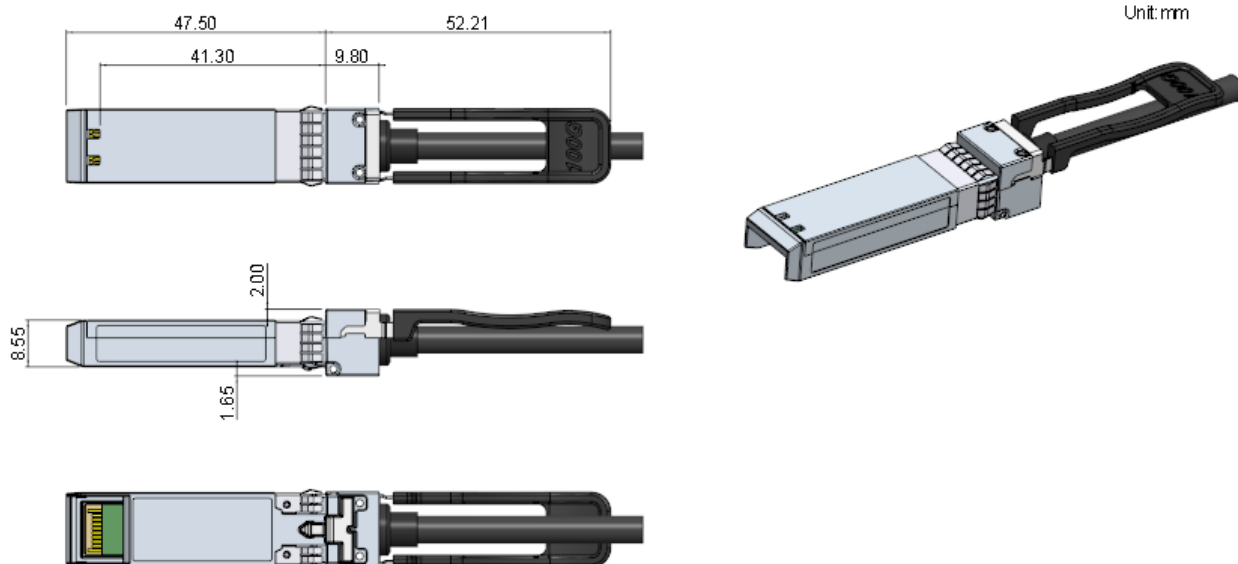
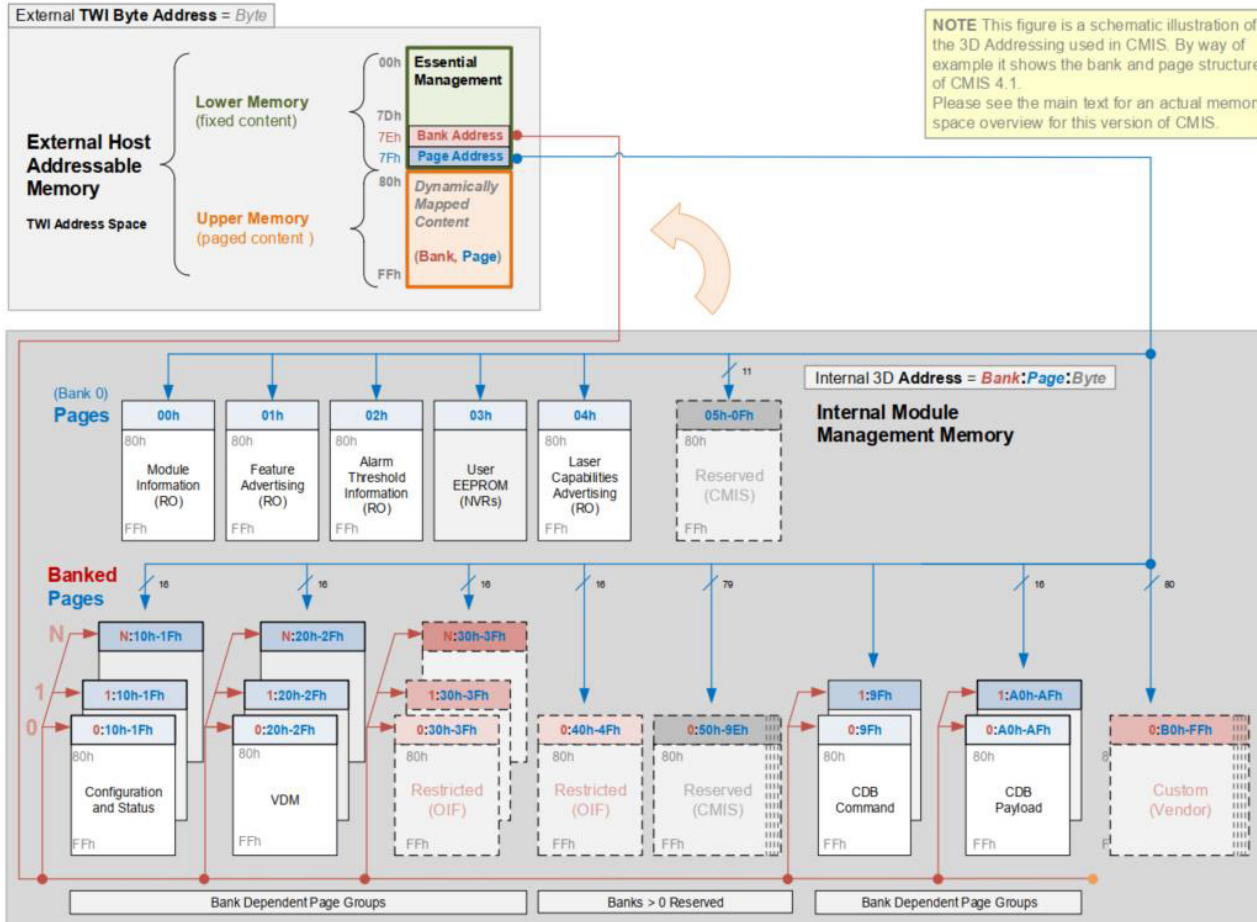


Figure 2 SFP112 to SFP112 Direct Attached Cable Assembly Wiring

Mechanical Specifications



Memory Map information (CMIS Version)



Lower Memory Overview

Address	Size	Subject Area	Description
0-3	4	ID and Status Area	Module ID from SFF8024 list, version number, Type and status Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h1Fh
8-13	6	ModuleLevel Flags	All flags that are not lane or data path specific
14-25	12	ModuleLevel Monitors	Monitors that are not lane or data path specific
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	ModuleLevel Flag Masks	Masking bits for the ModuleLevel flags
37-38	2	CDB Status Area	Status of most recent CDB command

39-40	2	Module Firmware Version	Module Firmware Version
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

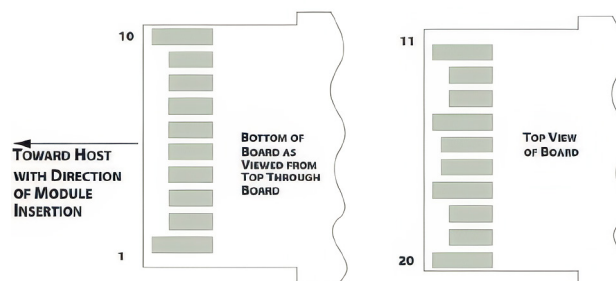
Note: For the above, refer to Common Management Interface Specification Rev5.0.

SFP112 PIN Function Definitions

Pin	Logic	Symbol	Description
1		VeeT	Module Transmitter Ground
2	LVTTL-O	Tx_Fault	Module Transmitter Fault
3	LVTTL-I	Tx_DIS	Transmitter Disable; Active High Disable Transmitter Output
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data
5	LVTTL-I/O	SCL	2-Wire Serial Interface Clock
6		Mod_ABS	Module Absent, connected to VeeT or VeeR in the module
7	LVTTL-I	RS0	Rx Rate Select
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication
9	LVTTL-I	RS1	Tx Rate Select
10		VeeR	Module Receiver Ground
11		VeeR	Module Receiver Ground
12	CML-O	RD-	Receiver Inverted Data Output
13	CML-O	RD+	Receiver Non-Inverted Data Output
14		VeeR	Module Receiver Ground
15		VccR	Module Receiver 3.3V Supply
16		VccT	Module Transmitter 3.3V Supply
17		VeeT	Module Transmitter Ground
18	CML-I	TD+	Transmitter Non-Inverted Data Input
19	CML-I	TD-	Transmitter Inverted Data Input
20		VeeT	Module Transmitter Ground

SFP112 Electrical Pad Layout

For detail mechanical information, please refer to the related document of SFP MSA.



Disclaimer

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