

QSFP-DD 800G to QSFP-DD 800G ACC



0.5~2.0M

PVC Black

Key Features

- Support 8x106.25G PAM4
- 800G To 800G Data Rate
- 3.3V Power Supply
- Hot Pluggable
- Excellent SI Performance
- Maximum power consumption:<1.5W each end
- RoHS Compliance

Applications

- Data Center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices

Supported Standards

- QSFP-DD MSA
- QSFP-DD-Hardware-Rev7.0
- IEEE 802.3ck
- IEEE 802.3cd
- CMIS 5.x



Ordering Information

LFGG-QM1xxxC

QSFP-DD 800G to QSFP-DD 800G ACC – 0.5~2.0M

Ordering P/Ns	Description	Length	AWG	Cable	NOTE
LFGG-QM1xx5C	QSFP-DD 800G to QSFP-DD 800G ACC	0.5m	30 AWG	PVC Black	
LFGG-QM1x15C	QSFP-DD 800G to QSFP-DD 800G ACC	1.5m	28 AWG	PVC Black	
LFGG-QM1x20C	QSFP-DD 800G to QSFP-DD 800G ACC	2.0m	26 AWG	PVC Black	

xxx define ACC cable length

Description

The LFGG-QM1xxxC QSFPDD to QSFPDD 800G Active Redriver Copper Cable Assembly, meticulously designed for application in the telecommunications and data center sectors. It facilitates bidirectional transmission of 800Gb traffic per cable, accommodating 8 lanes of 100G PAM4. The cable adheres to the standardized QSFPDD800 form factor and complies rigorously with MultiSource Agreement (MSA) specifications.

Absolute Maximum Ratings

Parameter	Unit	Min.	Max.	Notes
Supply Voltage	V	-0.3	3.6	
Data Input Voltage	V	-0.3	3.6	
Control Input Voltage	V	-0.3	3.6	
Operating Temperature	°C	0	70	
Storage Temperature	°C	-40	+85	
Relative Humidity (NonCondensing)	%	5	85	

Operational Specification

Parameter	Unit	Min	Typical	Max	Notes
Supply Voltage (Vcc)	V	3.135	3.3	3.465	Per End
Power Consumption	W			1.5	Per End
Operating Case Temperature	°C	0		70	
Operating Relative Humidity	%	0		85	
Modulation Format		112G PAM4			
Bit Rate	Gbps	8x100 to 8x100G			

Electrical Characteristics

Parameter	Unit	Min	Typical	Max	Notes
Characteristic Impedance	ohm	90	100	110	
Time Propagation Delay (Informative)	ns			4.9	

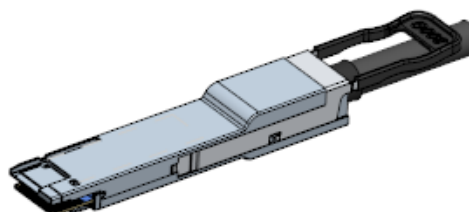
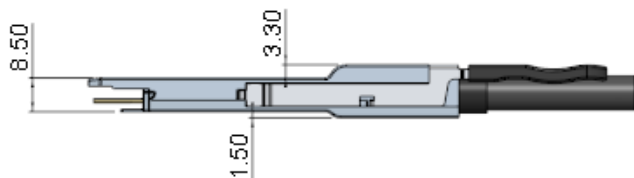
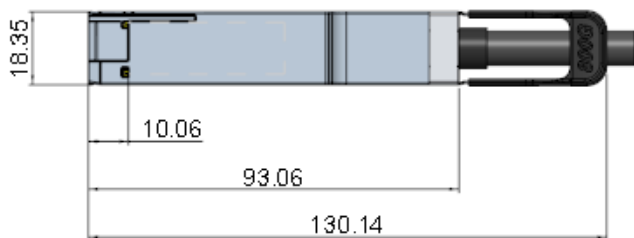
SI Performance

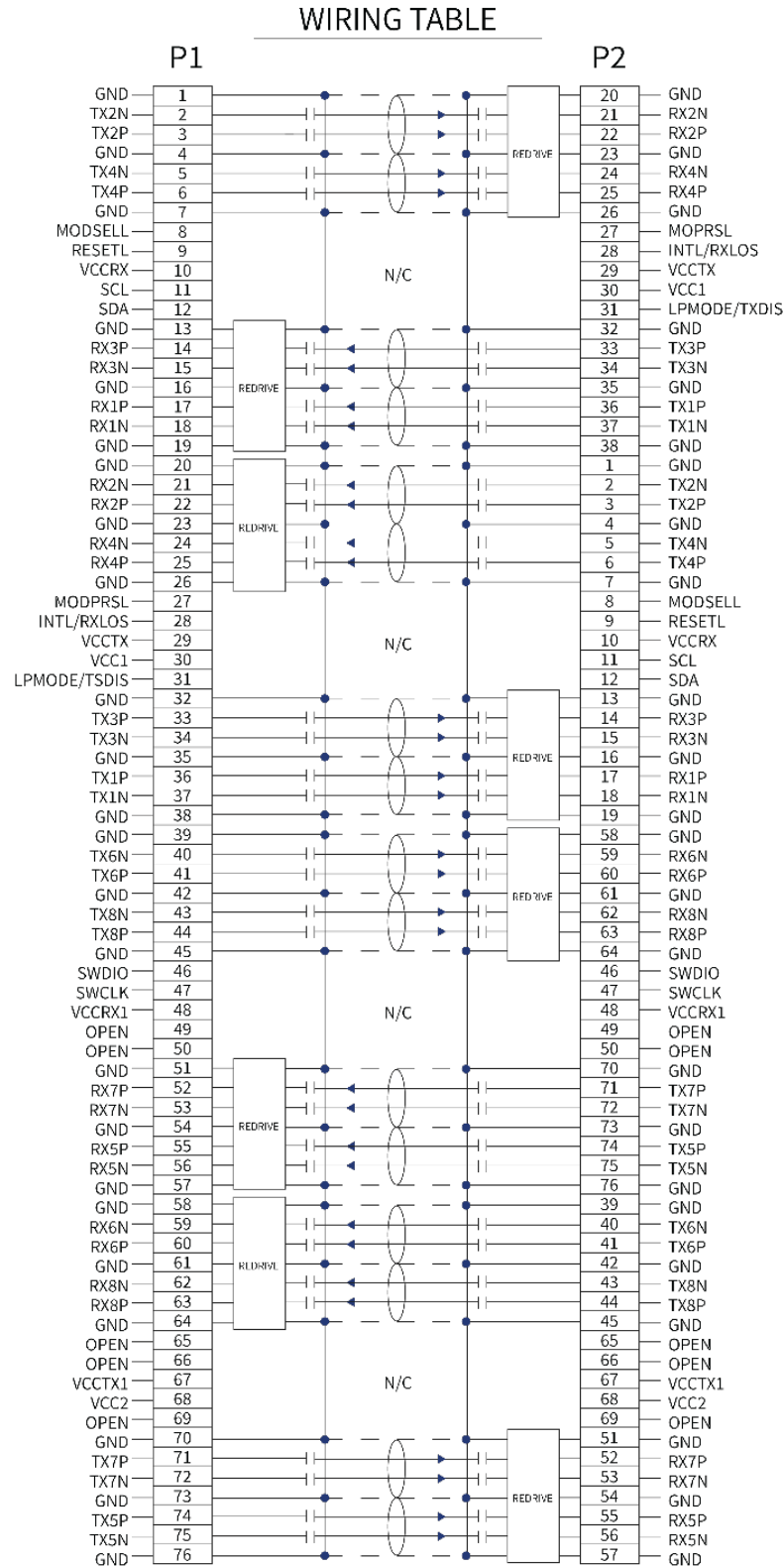
Item	Parameter	Require	Reference
1	ILdd Insertion loss at 26.56 GHz	19.75 dB (Max.)	IEEE 802.3ck Section 162.11.2
2	ILdd Insertion loss at 26.56 GHz	11 dB (Min.)	IEEE 802.3ck Section 162.11.2
3	ERL Minimum cable assembly	>8.25 dB*.	IEEE 802.3ck Section 162.11.3
4	RLcd Differential mode to common mode return loss	0.01GHz – 40GHz Equation (162–20)	IEEE 802.3ck Section 162.11.4
5	ILcd Differential mode to common mode insertion loss	0.01GHz – 40GHz Equation (162–21)	IEEE 802.3ck Section 162.11.5
6	RLcc Common mode to common mode return loss	0.01GHz – 40GHz Equation (162–22)	IEEE 802.3ck Section 162.11.6
7	COM	3dB (Min.)	IEEE 802.3ck Section 162.11.7

*Cable assemblies with a com greater than 4 dB are not required to meet minimum ERL

Mechanical Specifications

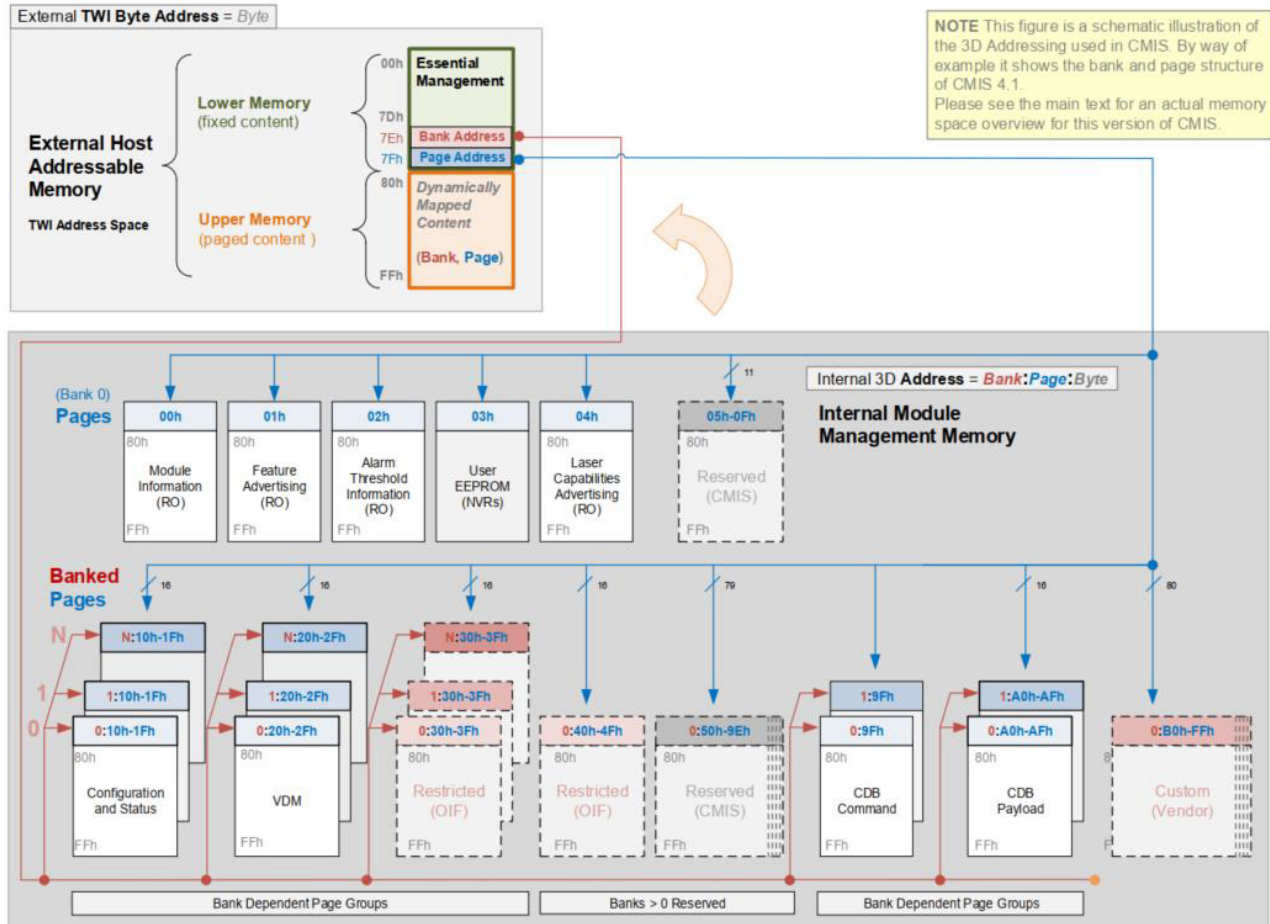
Unit:mm



Cable Wiring


QSFPDD to QSFPDD 800G Active Redriver Cable assembly Wiring

Memory Map information (CMIS Version)



Lower Memory Overview

Address	Size	Subject Area	Description
0-3	4	ID and Status Area	Module ID from SFF8024 list, version number, Type and status Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	ModuleLevel Flags	All flags that are not lane or data path specific
14-25	12	ModuleLevel Monitors	Monitors that are not lane or data path specific
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	ModuleLevel Flag Masks	Masking bits for the ModuleLevel flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version

41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

Page 00h Overview

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128221
223-255	33	Custom Info NV	

Note: For the above, refer to Common Management Interface Specification Rev5.0.

QSFP-DD PIN Function Definitions

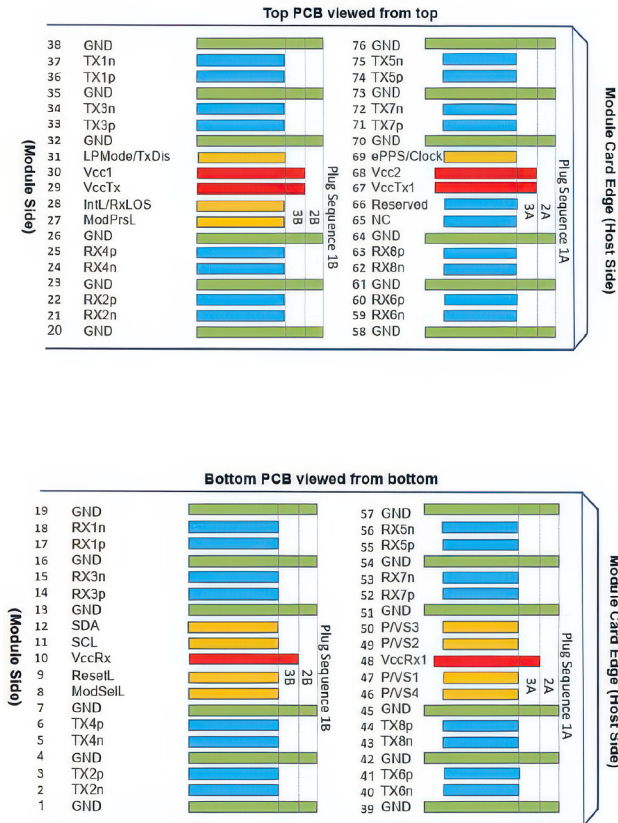
Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCOMS-I/O	SCL	TWI Serial Interface Clock
12	LVCOMS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output

25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RxLOSL	Interrupt/optional RxLOS
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMODE/TxDis	Low Power Mode/optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45		GND	Ground
46	LVCOMS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCOMS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
48		VccRx1	3.3V Power Supply

49	LVC MOS/CML-I	P/VS2	Programmable/Module Vendor Specific 2
50	LVC MOS/CML-I	P/VS3	Programmable/Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connect
66		Reserved	For future use
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69	LVCOMS-I	ePPS/Clock	1PPS PTP clock or reference clock input
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76		GND	Ground

QSFP-DD Electrical Pad Layout

For detail mechanical information, please refer to the related document of QSFP-DD MSA.



Disclaimer

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